

Performance Evaluation of Scientific Applications on POWER8

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Outline

- POWER8 architecture intro
- Micro benchmarks
 - STREAM memory bandwidth
 - OpenMP overheads
- Scientific HPC applications
 - LBM Lattice Boltzmann method for fluid dynamics
 - NEST Neuroscience network simulator
 - MAFIA subspace clustering data analysis tool



POWER8 chip architecture

3.42 GHz core frequency10 cores per socket (max 12)core architecture:

POWER ISA v2.07 8-way SMT 2xFXU, 2xLSU, 2xLU 2xVMX, 4xFPU







Memory hierarchy of POWER8





STREAM benchmark

with 2 streams

сору	c[i] =	a[i];
scale	b[i] =	s*c[i];

with 3 streams

sum	a[i] =	= b[i]+c[i];
triad	a[i] =	= s*b[i]+c[i];

efficient prefetching expected



STREAM memory traffic - copy





STREAM performance

Mitglied der Helmholtz-Gemeinschaft





OpenMP overheads

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Lattice Boltzmann method

Fluid dynamics

- discrete sampling of positions and velocities
- complex and irregular structures
- multi-phase flow possible



Example: Rayleigh-Taylor instability



Lattice Boltzmann method – D2Q37

- two kernels:

collide (6200 FP/lattice site)
propagate (BW limited)
on most platforms $t_{\text{collide}} >> t_{\text{propagate}}$

- high degree of parallelism
- high arithmetic intensity





LBM D2Q37 – performance





MAFIA

a parallelized algorithm to identify subspace clusters in high dimensional spaces

kernel: pcount bitwise &





Adinetz et al., Euro-Par'13 Proceedings, pp 838-849



MAFIA – performance





NEST – NEural Simulation Tool

- discrete event simulator on an a distributed graph
- uses domains-specific interpreter language (SLI)
- stochastic input
- hybrid parallelization with M×T virtual processes
- *n*=9375 neurons per MPI process
- dry-run mode for *M* processes
- kernels:
 - neuron update (some FP-ops)
 - spike delivery (dominant)





Brette et al. J Comp. Neuroscience Vol 23, 3 (2007)



NEST – total runtime

- control the binding of threads to cores
- dry-run mode with M=512 and M=16,384



use 160/T as stride



NEST – spike delivery

total amount of work fitted to $C = c_0 + c_1 MT + c_2 MT^2$





NEST – potential for improvement

- Each of *T* threads runs through *MT* buffer elements in the spike delivery kernel, avoiding the c₂ *MT*² component would improve thread-scalability
- Instructions per cycle throughput benefits from SMT8
- Needs deeper understanding



Summary

- LBM and MAFIA benefit from vectorization and instruction-level parallelism
- NEST benefits from SMT8, needs restructuring
- POWER8 suitable as host CPU in GPU-accelerated system



Outlook

POWER8 with GPUs

installed – porting in progress