

Prof. Doron A. Peled

Department of Computer Science
Bar Ilan University
Ramat Gan, 52900
Israel
Phone: + (972)(3)531-8765
email: doron.peled@gmail.com

Research Interests

Formal methods, formal verification, model-checking, software testing, software engineering, mathematical logic, automata and formal languages, semantics of programming languages, concurrency theory, software synthesis.

Education

D.Sc., The Technion, Israel Institute of Science, Department of Computer Science, supervisors: Prof. Shmuel Katz and Prof. Amir Pnueli. Research title: ‘Verification Methods in Temporal Logics’, 1991.

M.Sc., The Technion, Israel Institute of Science, Department of Computer Science, supervisor: Prof. Shmuel Katz. Research title: ‘Interleaving Set Temporal Logic’, 1987.

B.Sc., *cum lauda*, The Technion, Israel Institute of Science, Department of Computer Science, 1984.

Awards and Honors

- President’s list 1984.
- Gutwirt Excellency, Technion 1985.
- Full scholarship, 1985–1987.
- EASST (European Association of Software Science and Technology) *Best Software Science Paper* presented at the European Joint Conference on Theory and Practice of Software (ETAPS) 2001, April 2-6, Genova, Italy.

Research grants

NSF ITR Award (with A.E. Emerson, B. Goldberg, A. Pnueli, A.P. Sistla, L. Zuck), 2003-2006. This serves as a grant of \$466,000 for a period of 3 years for this group of researchers.

ISF grant “Synthesis of programs using combination of verification and genetic programming”, award 1262/09. Annual award of \$69,077 per year for 3 years, 2009-2012.

Professional Appointments

2011 – present MarktOberDorf Summer School co-director (with Prof. Manfred Broy), Orange Series (Software and System Safety).

April 2006 – present Full Professor of Computer Science, Bar Ilan University, Ramat Gan, Israel.

September 2002 – September 2008 Chair in Software Engineering (Full Professor), The University of Warwick, UK (on leave of absence).

September 2001 – September 2002 Associate Prof. Department of Electrical and Computer Engineering (tenured), The University of Texas at Austin.

July 1999 – July 2006 Adjunct Prof. Department of Computer Science, Carnegie Mellon University.

January–April 1998: Visiting associate professor, Carnegie Mellon University, Pittsburgh, USA. Teaching a course on *Analysis of Software Artifacts*.

1992– September 2001: Bell Laboratories. Member of Technical Staff. Research in the areas of verification and concurrency and development of software analysis tools.

September 1991–August 1992: Post-doctorate position at the University of Warwick, England. Research in the areas of program verification and fault-tolerance, teaching a course on *introduction to complexity*.

1987–1991: Military Service (overlapping with D.Sc. studies). Designing and developing expert systems, communication and database systems. Taught AI, Prolog courses.

1984–1987: Teaching assistant in the Technion, Israel Institute of Technology, faculty of Computer Science. Courses taught: Introduction to programming, Program verification, Semantics of programming languages, Programming languages, File systems.

Supervision

- Hongyang (Foster) Qu, Graduated November 2005 (Phd).
- Gal Katz, Graduated November 2007 (MSc). Will finish Phd in 2012.

Postdoc advising

- Blaise Genest, graduated Paris 7.
- Paola Spoletini, graduated Milano.
- Edith Elkind, graduated Princeton.

Summer Students (at Bell Labs)

- Anca Muscholl, Graduated Univ. of Stuttgart.
- Zhendong Su, Graduated Berkeley.
- Natasha Sharygina, Graduated Univ. of Texas, Austin.
- Alex Groce, Graduating CMU.
- Ching-Tsun Chou, Graduated UCLA.
- Girish Bhat, Graduated Stony Brook.

Journal Papers

1. S. Katz, D. Peled, Interleaving Set Temporal Logic, *Theoretical Computer Science*, 75 (1991) 21–43.
2. S. Katz, D. Peled, Defining Conditional Independence Using Collapses, *Theoretical Computer Science*, 101(1992), 337–359.
3. S. Katz, D. Peled, Verification of Distributed Programs Using Representative Interleaving Sequences, *Distributed Computing*, 6(1992), 107–120.
4. D. Peled, A. Pnueli, Proving Partial Order Properties, *Theoretical Computer Science*, 126(1994), 143–182.
5. M. Joseph, D. Peled, A Compositional Framework for Fault Tolerance by Specification Transformation, *Theoretical Computer Science*, 128(1994), 99–125.
6. D. Peled, Combining Partial Order Reductions with On-the-fly Model-Checking, *Journal of Formal Methods in Systems Design*, 8 (1996), 39–64.
7. D. Peled, On Projective and Separable Properties, *Theoretical Computer Science*, 186(1-2), 135–155.
8. R. Alur, G. Holzmann, D. Peled, An Analyzer for Message Sequence Charts, *Software: Concepts and Tools*, 17 (1996), 70–77.
9. P. Godefroid, D. Peled, M. Staskauskas, Using Partial Order Methods in the Formal Validation of Industrial Concurrent Programs, *IEEE, Transactions on Software Engineering*, 22 (1996), 496–507.
10. D. Peled, Th. Wilke, P. Wolper, An Algorithmic Approach for Checking Closure Properties of Temporal Logic Specification and ω -Regular Languages, *Theoretical Computer Science*, TCS 195(2): 183–203 (1998).
11. D. Peled, Th. Wilke, Stutter-Invariant Temporal Properties are Expressible without the Nexttime Operator, *Information Processing Letters* 63 (1997), 243–246.
12. R. Gerth, R. Kuiper, D. Peled, W. Penczek, A Partial Order Approach to Branching Time Logic Model Checking, *Information and Computation*, 150(2), 132–152, 1999.

13. C.T. Chou, D. Peled, Verifying a Model-Checking Algorithm, *Journal of Automated Reasoning* 23(3), 1999, 265–298.
14. D. Peled, Directions in Software Verification: User Interfaces for Formal Methods, a position paper, in E. Clarke, J. Wing (eds.), *ACM Workshop on Strategic Directions in Computing Research*, Formal Methods Working Group, 1996, *ACM Computing Surveys* 28(4es).
15. E.M. Clarke, O. Grumberg, M. Minea, D. Peled, State Space Reduction using Partial Order Techniques, *journal of Software Tools for Technology Transfer*. 2 (1999), 279-287.
16. G. Bhat, D. Peled, Adding Partial Orders to Linear Temporal Logic, *Fundamenta Informatica* 36(1):1–21(1998).
17. R. Alur, D. Peled, Undecidability of Partial Order Logics, *Information Processing Letters*, 69(1999) 137–143.
18. R. Alur, K. McMillan, D. Peled, Model-checking of Correctness Conditions for Concurrent Objects, *Information and Computation*, 166(2000), 167–188.
19. D. Peled, I. Kokkarinen, A. Valmari, Relaxed Visibility Enhances Partial Order Reduction, *Formal Methods in System Design*, 19(2001), 275–289.
20. R. Alur, K. Etessami, S. La-Torre, D. Peled, Parametric Temporal Logic for ‘Model Measuring’, Accepted to *ACM Transactions on Computational Logic*, Volume 2(3), 388–407, 2001.
21. R. Kurshan, M. Minea, V. Levin, D. Peled, H. Yenigun, Combining software and hardware verification techniques, *Formal Methods in System Design*, 21(3), 251-280, 2002.
22. D. Peled, M. Yannakakis, M.Y. Vardi, Black Box Checking, *Journal of Automata, Languages and Combinatorics*, Volume 7, 2002, 225-246.
23. R. Alur, K. McMillan, D. Peled, Deciding Global Partial-Order Properties, *Formal Methods in System Design*, 26 (2005), 7–25.
24. E. Gunter, A. Muscholl, D. Peled, Compositional Message Sequence Charts, *journal of Software Tools for Technology Transfer*. Volume 5, 2003, 78-89.
25. E. Gunter, D. Peled, Model Checking, Testing and Verification Working Together, *Journal of Formal Aspects of Computing*, 17 (2), 201-221, 2005.
26. A. Groce, D. Peled, M. Yannakakis, Adaptive Model Checking, *Logic Journal of the IGPL* 14(5), 2006, 729-744.
27. D. Peled, H. Qu, Enforcing Concurrent Temporal Behaviors, *International Journal on Foundations of Computer Science* 17(4), 2006, 743-762.
28. S. Bensalem, D. Peled, H. Qu, S. Tripakis, Automatic Generation of Path Conditions for Timed Systems, *Theoretical Computer Science Theoretical Computer Science*, 404, 2008 275-292.

29. D. Bosnacki, E. Elkind, B. Genest, D. Peled, On Comutativity Based Edge Lean Search, *Journal of Annals of Math and AI*, 56(2), 2009, 187-210.
30. P. Niebert, Efficient Model Checking for LTL with Partial Order Snapshots, *Theoretical Computer Science*, Volume 410, No. 42, 2009, 4180-4189.
31. E. Elkind, B. Genest, D. Peled, P. Spoletini, Qualifying the Discord: Order Discrepancies in Message Sequence Charts, *Journal of Foundations of Computer Science*, 21(2), 2010, 211-233.
32. A. Basu, S. Bensalem, D. Peled, J. Sifakis, Priority Scheduling of Distributed Systems based on Model Checking, *Formal Methods in System Design*, 39(3), 229–245, 2011.

Proceedings Papers

1. S. Katz, D. Peled, Interleaving Set Temporal Logic, *PODC'97, 6th Annual ACM Symposium on Distributed Computing*, 1987, 190–198, Vancouver, BC, Canada.
2. S. Katz, D. Peled, An Efficient Verification Method for Parallel and Distributed Programs, *Workshop on Linear Time, Branching Time and Partial Order in Logics and Models for Concurrency*, LNCS 354, Springer, 1988, 489-507, Noordwijkerhout, The Netherlands.
3. D. Peled, A. Pnueli, Proving Partial Order Liveness Properties, in M. S. Paterson (ed), *Proceedings ICALP'90*, LNCS 443, Springer, 1990, 553–571, Warwick University, England.
4. S. Katz, D. Peled, Defining Conditional Independence Using Collapses, *Semantics for Concurrency, Workshop in Computing Series*, Springer, 1990, 262–280, Leicester, UK.
5. D. Peled, S. Katz, A. Pnueli, Specifying and Proving Serializability in Temporal Logic, *LICS'91, 6th Symposium on Logic in Computer Science*, IEEE 1991, 232–244, Amsterdam, The Netherlands.
6. D. Peled, Sometimes “Some” Is as Good as “All”, *CONCUR'92, 3rd International Conference on Concurrency Theory*, LNCS 630, Springer, 1992, 192-206, Stony Brook, NY, USA.
7. D. Peled, All from One, One from All: on Model Checking using representatives, *CAV'93, 5th International Conference on Computer Aided Verification*, LNCS 697, Springer, 1993, 409–423, Elounda, Greece.
8. D. Peled, On Projective and Separable Properties, *Colloquium on Trees in Algebra and Programming*, LNCS 787, Springer, 1994, 291-307, Edinburgh, Scotland.
9. M. Joseph, D. Peled, A Compositional Framework for Fault Tolerance by Specification Transformation, *PARLE'93, 5th International Conference on Parallel Architectures and Languages Europe*, LNCS 694, Springer, 1993, 173–184. Munich, Germany.

10. D. Peled, Combining Partial Order Reductions with On-the-fly Model-Checking, *CAV'94, 6th International Conference on Computer Aided Verification*, LNCS 818, Springer, 377-390, 1994, Stanford, CA, USA.
11. M. Kwiatkowska, D. Peled, W. Penczek, A Hierarchy of Partial Order Temporal Properties, *First International Conference on Temporal Logic, ICTL'94*, LNCS 827, Springer, 398-414, 1994, Bonn, Germany.
12. G.J. Holzmann, D. Peled, An Improvement in Formal Verification, *FORTE'94, Formal Description Techniques 1994*, Chapman & Hall, 197-211, 1994, Bern, Switzerland.
13. R. Gerth, R. Kuiper, D. Peled, W. Penczek, A Partial Order Approach to Branching Time Logic Model Checking, *ISTCS'95, 3rd Israel Symposium on Theory on Computing and Systems*, 130-139, IEEE, 1995, Tel Aviv, Israel.
14. R. Alur, D. Peled, W. Penczek, Model-Checking of Causality Properties, *LICS'95, 10th Symposium on Logic in Computer Science*, IEEE, 1995, 90-100, San Diego, CA, USA.
15. D. Peled, W. Penczek, Using Asynchronous Büchi Automata for Efficient Model-Checking of Concurrent Systems, *PSTV'95, Protocol Specification Testing and Verification*, 315-330, Chapman & Hall, 1995, Warsaw, Poland.
16. R. Gerth, D. Peled, M.Y. Vardi, P. Wolper, Simple On-the-fly Automatic Verification of Linear Temporal Logic, *PSTV95, Protocol Specification Testing and Verification*, 3-18, Chapman & Hall, 1995, Warsaw, Poland.
17. P. Godefroid, D. Peled, M. Staskauskas, Using partial-order methods in the formal validation of industrial concurrent programs, *ISSTA'96 International Symposium on Software Testing and Analysis*, 1996, ACM Press, 261-269, San Diego, CA, USA.
18. C.T. Chou, D. Peled, Verifying a Model-Checking Algorithm, *TACAS'96, Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 1055, Springer, 1996, 241-257, Passau, Germany.
19. R. Alur, G.J. Holzmann, D. Peled, An Analyzer for Message Sequence Charts, *TACAS'96, Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 1055, Springer, 1996, Passau, Germany, March 1996, 35-48.
20. D. Peled, Partial Order Reduction: Linear and Branching Temporal Logics and Process Algebras, *POMIV'96, Partial Orders Methods in Verification*, American Mathematical Society, AMS DIMACS Series, 1996, Princeton, NJ, USA, 233-258.
21. R. Alur, K. McMillan, D. Peled, Model-checking of Correctness Conditions for Concurrent Objects, *LICS96, 11th IEEE Symposium on Logic in Computer Science*, 1996, 219-228, New Brunswick, NJ, USA.
22. G. Holzmann, D. Peled, M. Yannakakis, On Nested Depth First Search, *Second SPIN Workshop*, 1996, AMS DIMACS series, 1997, Piscataway, NJ, USA, 23-32.

23. G.J. Holzmann, D. Peled, The State of Spin, *CAV'96. 8th International Conference on Computer Aided Verification*, Springer, LNCS 1102, New Brunswick, NJ, USA, 1996, 385–389.
24. D. Peled, T. Wilke, P. Wolper, An Algorithmic Approach for Checking Closure Properties of ω -Regular Languages, *CONCUR'96, International Conference on Concurrency Theory*, Pisa, Italy, LNCS 1119, Springer, 1996, 596–610.
25. D. Peled, Partial Order Reduction: Model-Checking using Representatives, *MFCS'96, 21st International Symposium on Mathematical Foundations of Computing Science*, Cracow, Poland, LNCS 1113, Springer 1996, 93–112.
26. E.A. Emerson, S. Jha, D. Peled, Combining Partial Order and Symmetry Reduction, *TACAS'97, Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 1217, Enschede, The Netherlands, April 1997, 19–34.
27. V. Levin, D. Peled, Verification of Message Sequence Charts via Template Matching, *TAPSOFT (FASE)'97, Theory and Practice of Software Development*, Lille, France, LNCS 1214, 652–666.
28. G. Bhat, D. Peled, Adding Partial Orders to Linear Temporal Logic, *CONCUR'97*, Warsaw, Poland, July 1997, LNCS 1243, 119–134.
29. I. Kokkarinen, D. Peled, A. Valmari, Relaxed Visibility Enhances Partial Order Reduction, *CAV'97*, June 1997, Israel, LNCS 1254, 328–339.
30. D. Peled, Verification for Robust Specification, Conference on Theorem Proving in Higher Order Logic, LNCS 1275, Springer, August 1997, Murray Hill, NJ, USA, 231–241.
31. P.A. Abdulla, M. Kindahl, D. Peled, An Improved Search Strategy for Lossy Channel Systems, *PSTV/FORTE'97*, Osaka, Japan.
32. R.P. Kurshan, V. Levin, M. Minea, D. Peled, H. Yenigun, Verifying Hardware in its Software Context, *ICCAD'97*, San Jose, CA, USA, November 1997, 742–749.
33. R.P. Kurshan, V. Levin, M. Minea, D. Peled, H. Yenigun, Static Partial Order Reduction, with *TACAS'98, Workshop on Tools and Algorithms for the Construction and Analysis of Systems*, Lisbon, Portugal, LNCS 1384, 345–357.
34. A. Muscholl, D. Peled, Z. Su, Deciding Properties for Message Sequence Charts, *FoS-SaCS, Foundations of Software Science and Computation Structures*, Lisbon, Portugal, 1978, LNCS 1378, 226–242.
35. P.A. Abdulla, B. Jonsson, M. Kindahl, A General Approach to Partial Order Reductions in Symbolic Verification, *Computer Aided Verification 98*, LNCS 1427, Springer, Vancouver, BC, Canada, 1998, 379–390.
36. D. Peled, A Toolset for Message Sequence Charts, *Computer Aided Verification 98*, LNCS 1427, Springer, Vancouver, BC, Canada, 1998, 532–536.

37. R. Alur, K. McMillan, D. Peled, Deciding global partial-order properties, *ICALP'98*, Aalborg, Denmark, July, 1998, LNCS 1443, Springer, 41-52.
38. D. Peled, Ten Years of Partial Order Reduction, *Computer Aided Verification 98*, LNCS 1427, Springer, Vancouver, BC, Canada, 1998, 17–28.
39. E.L. Gunter, D. Peled, Path Exploration Tool, *TACAS'99, Workshop on Tools and Algorithms for the Construction and Analysis of Systems*, Amsterdam, The Netherlands, LNCS 1579, Springer, 405–419.
40. R. Alur, K. Etessami, S. La Torre, D. Peled, Parametric Temporal Logic for Model Measuring, *ICALP'99*, LNCS 1644, Springer, Prague, July 1999, 159–168.
41. S. Jha, D. Peled, Generalized Stuttering Equivalence, 1999 International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'99), Las Vegas, June 1999, 1054–1060.
42. A. Muscholl, D. Peled, Message Sequence Graphs and Decision Problems on Mazurkiewicz Traces, *Mathematical Foundations of Computer Science*, Szklarska Poreba, Poland, September 1999, LNCS 1672, Springer, 81–91.
43. D. Peled, M.Y. Vardi, M. Yannakakis, Black Box Checking, *FORTE/PSTV 1999, Formal Methods for Protocol Engineering and Distributed Systems*, Beijing, China, 225-240.
44. D. Peled, Formal methods for message sequence charts, *Proceedings of DSVV (Distributed Systems Validation and Verification)*, Taipei, Taiwan, 2000, E7-E12.
45. E.L. Gunter, R.P. Kurshan, D. Peled, PET: an interactive software testing tool, 12th International Conference on Computer Aided Verification, *CAV*, Chicago, IL, USA, 2000, LNCS 1855, 552–556.
46. E.L. Gunter, D. Peled, Using a mix of languages in formal methods: the PET system, *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'00)*, Las Vegas, NE, USA, 2000, 2981–2986.
47. D. Peled, Specification and Verification of Message Sequence Charts, *FORTE/PSTV 2000, Formal Methods for Protocol Engineering and Distributed Systems*, Pisa, Italy.
48. N. Sharygina, D. Peled, A combined testing and verification approach for software reliability, *Formal Methods Europe 2001*, LNCS 2021, 611–628.
49. E. Gunter, A. Muscholl, D. Peled, Compositional Message Sequence Charts, *TACAS (Tools and Algorithms for the Construction and Analysis of Systems) 2001*, Genova, Italy, LNCS 2031, 496–511.
50. L. Zuck, D. Peled, From model checking to a temporal proof, *The 8th International SPIN Workshop on Model Checking of Software (SPIN'2001)*, Toronto, Canada, LNCS 2057, Springer, 1–14.

51. A. Muscholl, D. Peled, From Finite State Communication Protocols to High-Level Message Sequence Charts, accepted to ICALP 2001, Greece, LNCS 2076, Springer, 720–731.
52. D. Peled, A. Pnueli, L. Zuck, From Falsification to Verification, Accepted to FST TCS 2001, India, LNCS 2245, Springer, 292–304.
53. E.L. Gunter, D. Peled, Temporal Debugging for Concurrent Systems, TACAS (Tools and Algorithms for the Construction and Analysis of Systems) 2002, Grenoble, France, LNCS 2280, Springer, 431–444.
54. A. Groce, D. Peled, M. Yannakakis, Adaptive Model Checking, TACAS (Tools and Algorithms for the Construction and Analysis of Systems) 2002, Grenoble, France, LNCS 2280, Springer, 357–270.
55. C. Eisner, D. Peled, Comparing Symbolic and Explicit Model Checking of a Software Systems, SPIN 2002, LNCS 2318, Springer, Grenoble, France, 230–239.
56. D. Peled, Specification and Verification Using Message Sequence Charts, Electronic notes in Theoretical Computer Science 65(2002).
57. A. Groce, D. Peled, M. Yannakakis, AMC: An Adaptive Model Checker, Computer Aided Verification 2002, Copenhagen, Denmark, July 2002, LNCS 2404, Springer, 521–525.
58. E. Gunter, D. Peled, Tracing the executions of concurrent programs, Workshop on Runtime Verification, Copenhagen, Denmark, July 2002, Electronic notes in Theoretical Computer Science, 70(4).
59. D. Peled, Model Checking and Testing Combined, ICALP 2003, LNCS 2719, Springer, 47–63.
60. D. Peled, H. Qu, Automatic Verification of Annotated Code, FORTE 2003, LNCS 2767, Springer, 127–143.
61. E. Gunter, D. Peled, Unit Checking: Symbolic Model Checking for a Unit of Code, International Symposium on Verification (theory and practice), LNCS 2772, Springer, Taormina, Italy, 2003, 250–270.
62. B. Genest, M. Minea, A. Muscholl, D. Peled, Specifying and Verifying Partial Order Properties using template MSCs, FOSSaCS (Foundation of Software Science and Computation Structures) 2004, LNCS 2987, Springer, 195–210.
63. B. Genest, A. Muscholl, D. Peled, Message Sequence Charts, 4th Advanced Course on Petri Nets 2003, LNCS 3098, Springer, 2004, 537–558.
64. H. Qu, D. Peled, Enforcing Concurrent Temporal Behaviors, 4th Workshop on Runtime Verification, Barcelona, Spain, 2004, Electronic Notes in Computer Science, Volume 133, 65–83.

65. B. Genest, D. Kuske, A. Muscholl, D. Peled, Snapshot Verification, TACAS (Tools and Algorithms for the Construction and Analysis of Systems) , LNCS 3440, springer-verlag, 2005, 510–525.
66. A. Muscholl, D. Peled, Deciding Properties of Message Sequence Charts, Scenarios: Models, Transformations and Tools 2003, LNCS 3466, Springer, 43-65.
67. S. Bensalem, D. Peled, H. Qu, S. Tripakis, Generating Path Conditions for Timed Systems, LNCS 3771, Springer, 5th international conference on Integrated Formal Methods, Eindhoven, The Netherlands, 2005, 5–19.
68. P. Niebert, D. Peled, Efficient Model Checking for LTL with Partial Order Snapshots, TACAS 2006, Vienna, Austria, LNCS 3926, Springer, 272–286.
69. E. Elkind, B. Genest, D. Peled, H. Qu, Grey-Box Checking, Forte 2006, Paris, LNCS 4229, Springer, 420–435.
70. E. Elkind, B. Genest, D. Peled, Detecting Races in Ensembles of Message Sequence Charts, TACAS 2007, Braga, Portugal, LNCS 4424, Springer, 420–434.
71. D. Bosnacki, E. Elkind, B. Genest, D. Peled, On Commutativity Based edge Lean Search, ICALP 2007, LNCS 4596, Wroclaw, Poland, 158–170.
72. E. Elkind, B. Genest, D. Peled, P. Spoletini, Quantifying the Discord: Order Discrepancies in Message Sequence Charts, LNCS 4762, ATVA 2007, Japan, 378-393.
73. S. Bensalem, D. Peled, H. Qu, S. Tripakis, L. Zuck, Test Case Generation for Ultimately Periodic Paths, HVC 2007, Haifa, Israel, LNCS 4899, 120–135.
74. G. Katz, D. Peled, Model Checking-Based Genetic Programming with an Application to Mutual exclusion, TACAS 2008, Budapest, Hungary, LNCS 4963, 141–156.
75. P. Niebert, D. Peled, A. Pnueli, Discriminative Model Checking, CAV (Computer Aided Verification) 2008, Princeton, NJ, LNCS 5123, 504-516.
76. G. Katz, D. Peled, Genetic Programming and Model Checking, Synthesizing New Mutual Exclusion Algorithms, ATVA 2008, Seoul, Korea, 33-47.
77. G. Katz, D. Peled, Model Checking Driven Heuristic Search for Correct Programs, MoChArt 2008, Petras, Greece, LNCS 5348, Springer, 122-131.
78. Ananda Basu, Saddek Bensalem, Doron Peled, Joseph Sifakis: Priority Scheduling of Distributed Systems Based on Model Checking. CAV 2009, LNCS 5643, Grenoble, France, 79-93.
79. G. Katz, D. Peled, Synthesizing Solutions to the Leader Election Problem using Model Checking and Genetic Programming, HVC 2009, Haifa, Israel, LNCS 6405, Springer, 117–132.
80. G. Katz, D. Peled, Code Mutation in Verification and Automatic Code Correction, TACAS 2010, Cyprus, LNCS 6015, Springer, 435-450.

81. S. Bensalem, D. Peled, J. Sifakis, Knowledge based scheduling of distributed systems, *Esseys in Memory of Amir Pnueli*, LNCS 6200, 26-61.
82. S. Graf, D. Peled, S. Quinton, Achieving distributed control through model checking, *CAV 2010*, LNCS 6174, Edinburgh, UK, 396-4009.
83. S. Bensalem, M. Bozga, S. Graf, D. Peled, S. Quinton, Methods for knowledge based controlling of distributed systems, *ATVA 2010*, Singapore, LNCS 6252, Springer, 52-66.
84. G. Katz, D. Peled, MCGP: A Software synthesis tool based on model checking and genetic programming, *ATVA 2010*, Singapore, LNCS 6252, 259-364.
85. G. Katz, D. Peled, S. Schewe, Synthesis of Distributed Control Through Accumulated Knowledge, *CAV 2011*, Snowbird, Utah, LNCS 6806, Springer, 510-525.
86. S. Graf, D. Peled, S. Quinton, Monitoring Distributed Systems using Knowledge, *FORTE-FMOODS 2011*, Reykjavik, Iceland, LNCS 6722, Springer, 183-197.
87. S. Bensalem, A. Legay, A. Griesmeyer, T. H. Nguyen, D. Peled, Efficient Deadlock Detection for Concurrent Systems, Accepted to Memocode 2011, Cambridge, England.
88. D. Peled, S. Schewe, Practical Distributed Control, *Infinity 2011*, Taipei, Taiwan, 2-19.
89. G. Katz, D. Peled, S. Schewe, The Buck Stops Here: Order, Chance and Coordination in Distributed Control, *ATVA 2011*, LNCS 6996, Taipei, Taiwan, 422-431.

Book Chapters

- Model Checking Using Automata Theory, in K. Inan (ed.), *Verification of Digital and Hybrid Systems*, Springer.
- Partial Order Reductions, in K. Inan (ed.), *Verification of Digital and Hybrid Systems*, Springer.
- Model Checking, with Paola Spoletini and Patricio Pelliccione, in *Encyclopedia of Computer Science*, Benjamin Wah (ed.), John Wiley.
- Model Checking, in M. Broy, Ch. Leuxner, C.A.R. Hoare (eds), *Software and Systems Safety*, IOS Press.

Patents

1. On the fly model checking with partial order state space reduction, US patent 5,615,137, with Gerard Holzmann.
2. Message Sequence Chart Analyzer, US patent 5,812,145, with Gerard Holzmann.
3. Verifying hardware in its software context and vice-versa, US patent 6209120, European patent 98308795.8, with Robert P. Kurshan, Vladimir Levin, Marius Minea and Husnu Yenigun.

4. Static Partial Order Reduction, European Patent 98308793.3, US Patent 6,295,515, With Robert P. Kurshan, Vladimir Levin, Marius Minea and Husnu Yenigun.
5. Verification of Message Sequence Charts, US Patent, 6,346,879, with Gerard Holzmann.
6. Interactive software testing system and method 6,408,430, with Elsa Gunter.
7. Directly verifying a black box system, 6,526,544, with Moshe Vardi and Mihalis Yannakakis.

Books Authored:

- E.M. Clarke, O. Grumberg, D. Peled, *Model Checking*, December 1999, MIT Press, ISBN: 0-262-03270-8.
- D. Peled, *Software Reliability Methods*, Springer, July 2001, ISBN: 3-879-5106-7.

Conference Proceedings Edited (as program co-chair:

- *Partial Order in Verification*, with V. Pratt and G. Holzmann, *AMS DIMACS series*, 1997, ISBN: 0-8218-0579-7.
- *SPIN'96 proceedings*, with G. Holzmann, J.C. Gregoire, *AMS DIMACS series*, 1997, ISBN: 0-8218-0680-7.
- *11th International Conference on Computer Aided Verification (CAV'99) proceedings*, LNCS 1633, Springer, July 1999, ISBN: 3-540-66202-2.
- *22nd IFIP WG 6.1 International Conference on Formal Techniques for Networked and Distributed Systems - FORTE 2002*, Houston, Texas, USA, November 11-14, 2002, Volume 2529 in the Series Lecture Notes in Computer Science.
- *15th International Conference on Computer Aided Verification (CAV'04) proceedings*, LNCS 3114, Springer, July 2004,
- *3rd Automated Technology for Verification and Analysis*, International Symposium, ATVA 2005, Taipei, Taiwan, October 4-7, 2005, Lecture Notes in Computer Science 3707, Springer 2005.
- *9th conference on Verification, Model Checking and Abstract Interpretation*, VMCAI 2008, January 7-9, San Francisco, USA, LNCS 4905, Springer, 2008.

Professional Activities

- Program committee member, *CONCUR'93, Conference on Concurrency Theory*, Hildesheim, Germany.
- Program committee member, *CAV'96, Conference on Computer Aided Verification*, New Brunswick, NJ, USA.

- Program committee member, *ISTCS'96, Israel Symposium on the Theory of Computing and Systems*.
- Co-chair, *POMIV'96, Workshop on Partial Order Methods in Verification*, Princeton, NJ, USA.
- Co-chair, *SPIN'96, 2nd SPIN workshop*, Piscataway, NJ, USA.
- Program committee member, *CONCUR'97, Conference on Concurrency Theory*, Warsaw, Poland.
- Editorial board, *Journal of Formal Methods in System Design* (Kluwer).
- Program committee member, *TACAS'98, Workshop on Tools and Algorithms for the Construction and Analysis of Systems*, to be held in Lisbon, Portugal.
- Program committee member, *VISUAL'98, Workshop on Visualization Issues for Formal Methods*, to be held in Lisbon, Portugal.
- Program committee member, *LICS'98, Logic in Computer Science*, to be held in Indianapolis, Indiana.
- Program committee member, *CAV'98, Computer Aided Verification*, to be held in UBC, Vancouver, British Columbia, Canada.
- Program co-chair *CAV'99, Computer Aided Verification*, Trento, Italy.
- External Phd. examiner, Marius Minea, CMU, December 1999.
- Member, NSF Panel on software engineering, January 2000.
- Program committee member, *DSVV'2000* Taipei, Taiwan.
- Program committee member, *CAV'2000, Computer Aided Verification*, Chicago, IL.
- Program committee member, *SPIN'2000*, Stanford, CA.
- Program committee member, *TACAS'2001*, Genova, Italy.
- Program committee member, *FORTE/PSTV'2001*, Korea.
- Program committee member, *FATES'01*, Grenoble, France.
- Program committee member, *SPIN'2002*, Grenoble, France.
- Program co-chair *FORTE/PSTV'2002*, Houston, TX, USA.
- Program committee member, *LICS'2002*, Copenhagen, Denmark.
- Program committee member, *CAV'2002*, Copenhagen, Denmark.
- Program committee member, *FATES'02*, Brno, Czech Republic.

- Program Committee member, *CONCUR'03*, Marseille, France.
- Program committee member, *TACAS'03*, Warsaw, Poland.
- Program committee member, *FORTE'03*, Berlin, Germany.
- Program committee member, *CAV'03*, Boulder, Denver.
- Program committee member, *ATVA '03*, Taipei, Taiwan.
- Program committee member, *FORTE'04*, Spain.
- Program committee member, *AVoCS'04*, London, UK.
- Program Co-chair of *CAV'04*, Boston, MA.
- Program committee member, *ATVA '04*, Taipei, Taiwan.
- Program committee member, *FASE'05*, Edinburgh.
- Steering committee member, *ATVA*.
- Program Co-Chair of *ATVA '05*, Taipei, Taiwan.
- Program committee member, *CAV'05*, Edinburgh.
- Program committee member, *FATES'05*, Edinburgh.
- Program committee member, *RV'05*, Edinburgh.
- Program committee member, *ACSD 2006*, Turku.
- Program committee member, *FATES/RV 2006*, Seattle.
- Program committee member, *ATVA 2006*, Beijing.
- Program committee member, *ACSD 2007*, Bratislava.
- Program committee member, *ICALP 2007*, Wroclaw.
- Program committee member, *ATVA 2007*, Tokyo.
- Program committee member, *FORTE 2007*, Tallinn.
- Program committee member, *TESTCOM-FATES 2007*, Tallinn.
- Program committee member, *SPIN 2007*, Berlin.
- Organizer of *1st Israeli Verification Day*, Bar Ilan University, June 2007.
- Program co-chair *VMCAI 2008*, San Francisco.
- Program co-chair *MoChArt 2008*, Patras, Greece.

- Program committee member, *SPIN 2008*, Los Angeles.
- Program committee member, *FORTE 2008*, Tokyo, Japan.
- Program committee member, *TESTCOM-FATES 2008*, Tokyo, Japan.
- Program committee member, *ACSD 2008*, Xian, China.
- Program committee member, *ATVA 2009*, Macau.
- Program committee member, *ACSD 2009*, Augsburg.
- Program co-chair *RV 2009*, Grenoble, France.
- Program committee member, *TACAS 2010*, Cyprus.
- Program co-chair *TASE 2010*, Taipei, Taiwan.
- Program committee member, *CAV 2010*, Edinburgh, UK.
- Program committee member, *SPIN 2010*, Enschede, The Netherlands.
- Program committee member, *ICTSS 2010*, Natal, Brazil
- Program committee member, *TACAS 2011*, Saarbrücken, Germany.
- Program committee member, *SPIN 2011*, Snowbird, Utah.
- Program committee member, *ATVA 2011*, Taipei, Taiwan.
- Program committee member, *FMCAD 2011*, Austin, Texas.
- Program committee member, *ICTSS 2011*, Paris, France.
- Program committee member, *TACAS 2012*, Tallinn, Estonia.
- Program co-chair, *SYNT 2012*, Berkeley, California.

Invited talks, Tutorials

1. *Workshop on Temporal Logic in Specification*, Altrincham, UK, 1987.
2. *Workshop on Combining Compositionality and Concurrency*, Königswinter, Germany, March, 1988.
3. *Workshop on Linear Time, Branching Time and Partial Order in Logics and Models of Concurrency*, Noordwijkerhout, The Netherlands, 1988.
4. *Workshop on Non Interleaved Models and Logic*, Gustav Strassenman Institute, Bonn, Germany, March, 1992.
5. *Tutorial on Partial Order Model-Checking in Theory and Practice*, IFIP Symposium on Protocol Specification Testing and Verification, Vancouver B.C., Canada, 1994.

6. *MFCS'96, Conference on Mathematical Foundation of Computer Science*, Cracow, LNCS 1113, Springer, Poland, September 1996.
7. *DIMACS Workshop on Computational and Complexity Issues in Automated Verification*, New Brunswick, NJ, March 1996.
8. *Dimacs Workshop: Special Year on Logic and Algorithms - One Year Later*, Rutgers, NJ, USA, July 23-25, 1997.
9. *ASI Nato Summer School on Verification of Digital and Hybrid Systems*, 5/26-6/6, 1997, Antalya, Turkey.
10. *TPHOL'97, 10 International Conference on Theorem Proving in Higher Order Logic*, 19-22 August 1997, Murray Hill, NJ.
11. *A Workshop on Traces and Logic*, Technische Universität Dresden, November 3 - 5, 1997.
12. *Invited Tutorial on Partial Order Reduction*, Computer Aided Verification, 1998, UBC, Canada.
13. *International Conference on Parallel and Distributed Processing Techniques and Applications*, Las Vegas, NV, June 1999.
14. *Distributed Systems Validation and Verification*, Taipei, Taiwan, April 10-13, 2000.
15. *SAM 2000, 2nd workshop on SDL and MSC*, Grenoble, France, June 26-28, 2000.
16. *IBM Formal Verification Seminar 2000*, Haifa, Israel, August 15-17.
17. *2nd Workshop on Formal Design of Safety Critical Embedded Systems, FEMSYS 2001*, 21-23 March, 2001, Munich, Germany.
18. *Spin 2001 workshop*, May 19-20, May 2001, Toronto, Canada.
19. *Dutch Model Checking Day*, November 2001, Eindhoven, the Netherlands.
20. *SPIN 2002*, Grenoble, France, 2002.
21. *VISS 2002*, April 2002, Grenoble, France.
22. *RV 2002*, Invited talk, Kopenhagen, Denmark.
23. *ICALP 2003*, Distinguished lecture, Eindhoven, The Netherlands.
24. *AVoCS 2003*, Invited talk.
25. *ATVA 2003*, Distinguished lecture, Taipei, Taiwan.
26. *IFM 2005*, Invited talk, Eindhoven, The Netherlands.
27. *Movep 2006*, Invited talk, Bordeaux, France.

28. *ESSCaSS 2006*, Invited tutorial, Pedase, Estonia.
29. *Omega 2007*, Invited talk, Taipei, Taiwan.
30. *A-MOST 2009*, Keynote speaker, Denver, Colorado.
31. *Infinity 2011*, Keynote speaker, Teipei, Taiwan.

List of referees.

Prof. Parosh Abdulla Uppsala University, Sweden.

email: paroshit.uu.se

Prof. Christel Baier Technische Universität Dresden.

email: christel@tcs.inf.tu-dresden.de

Prof. Edmund M. Clarke Carnegie Mellon University.

email: emc@cs.cmu.edu

Prof. Moshe Vardi Rice University,

email: vardi@cs.rice.edu