FRIEDRICH-ALEXANDER
UNIVERSITÄT
ERLANGEN-NÜRNBERG

FACULTY OF ENGINEERING

Automatic Throughput and Critical Path Analysis of x86 and ARM Assembly Kernels

J. Laukemann, J. Hammer, G. Hager, G. Wellein

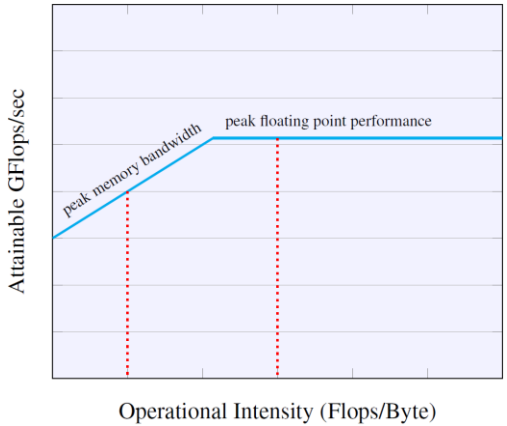
Overview

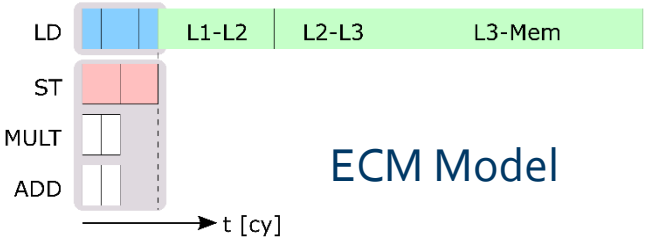
1. **Analytic Performance Modeling**
   Why?
   Assumptions & Related Tools
2. **Throughput & Latency - Nomenclature**
   Definition of Throughput, Critical Path and Loop-Carried Dependency
3. **OSACA: Automating the in-core model construction**
   Overview, Structure and Output
4. **Gauss-Seidel-Method Example**
5. **Future Work**

Performance Modeling for Loop Kernels

- **How fast can my kernel run *at best*?**
- **What are the relevant hardware bottlenecks?**
- **Apply simplified model of underlying hardware**
  - **In-core execution**
  - Data transfer
  - Combining execution and data transfer

Roofline Model





ECM Model

Performance Modeling for Loop Kernels

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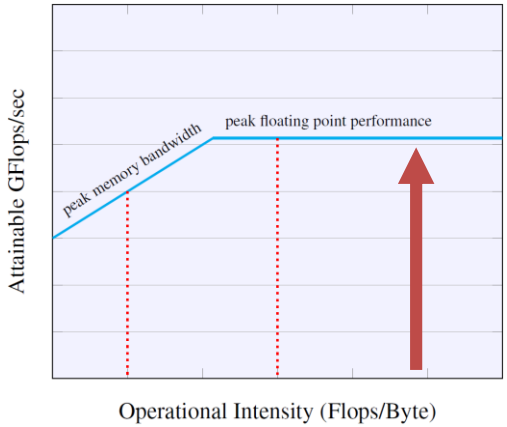
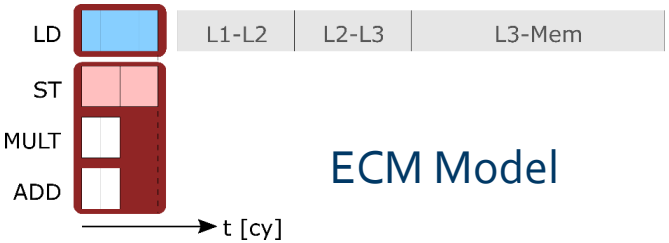




ECM Model

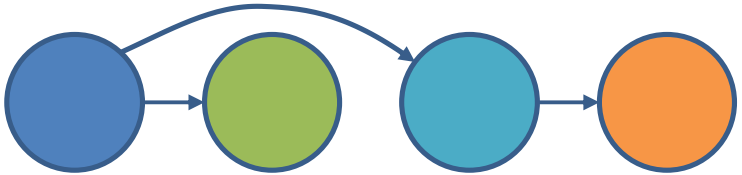
Assumptions & Related Tools

1. **All Data in L1**
2. **Average distribution of port scheduling**

	OSACA v0.2[1]	OSACA v0.3	IACA[2] (EoL)	LLVM-MCA[3]
Throughput	✓	✓	✓	✓
Critical Path	✗	✓	✗	😕
Loop-Carried Dependencies	✗	✓	✗	😕

[1] Presented at PMBS18
[2] Intel Architecture Code Analyzer (https://software.intel.com/en-us/articles/intel-architecture-code-analyzer)
[3] LLVM Machine Code Analyzer (https://llvm.org/docs/CommandGuide/llvm-mca.html)

Throughput & Latency



TP: 1 cy

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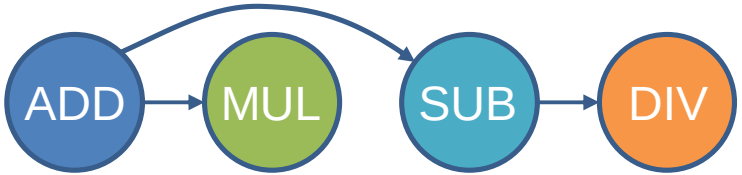
Throughput & Latency



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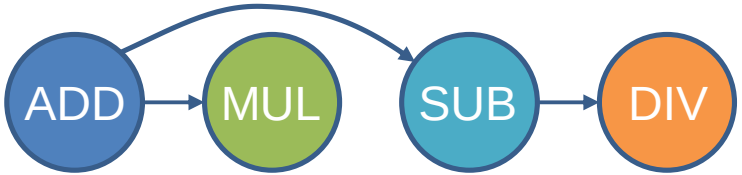

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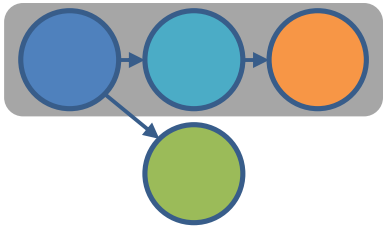

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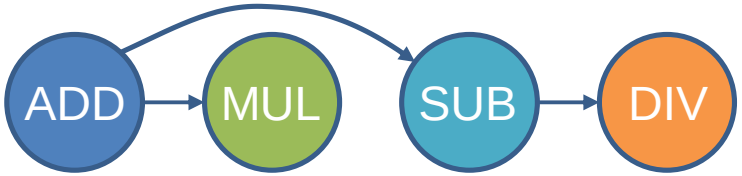

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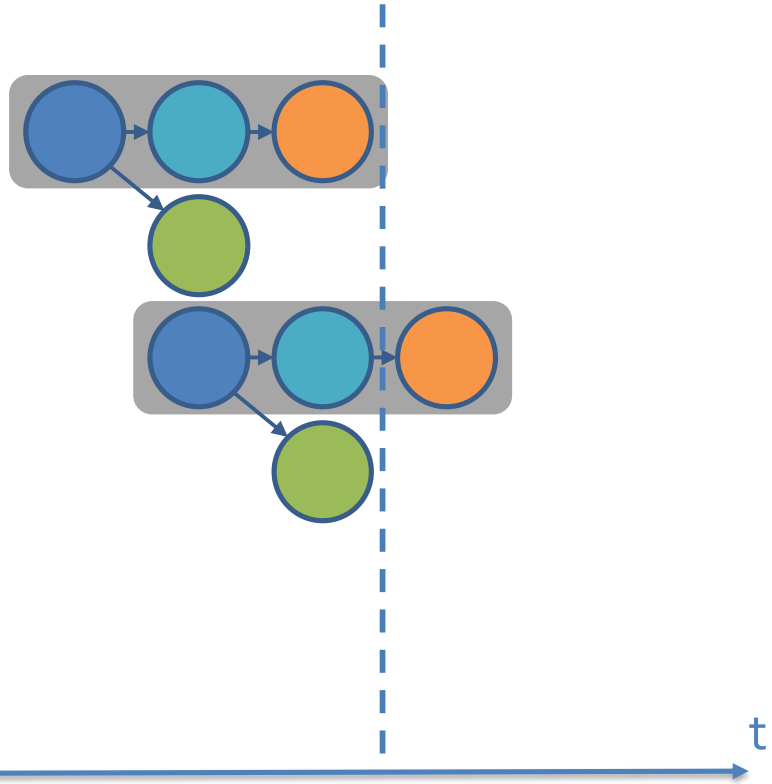

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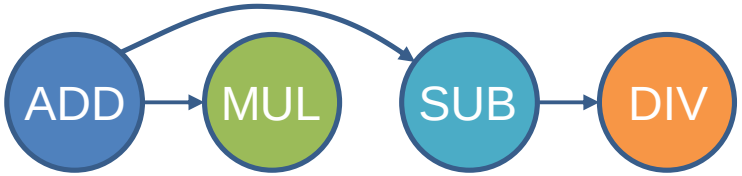

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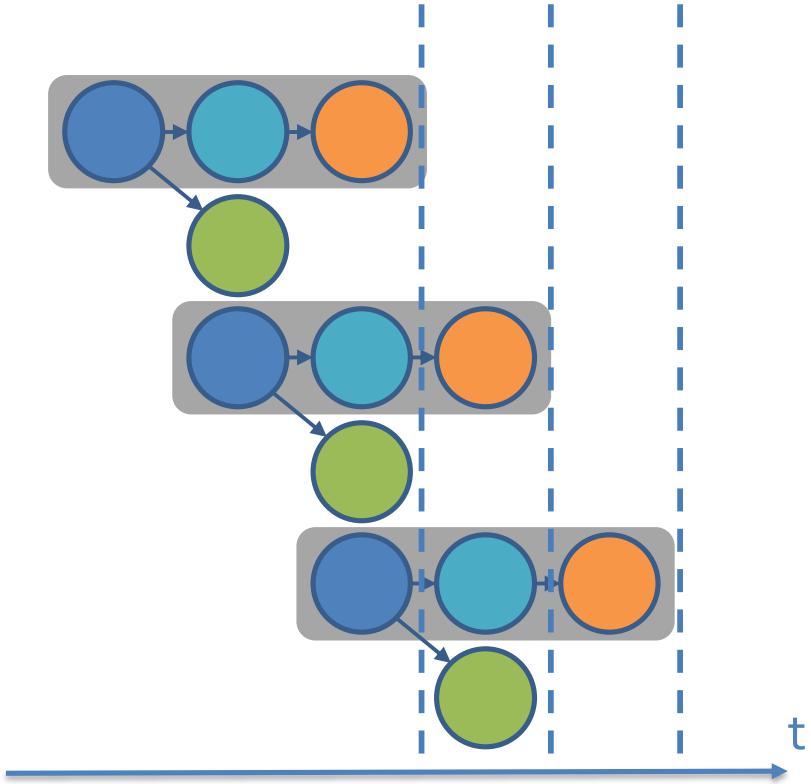

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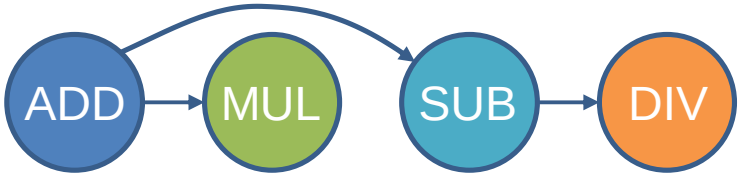

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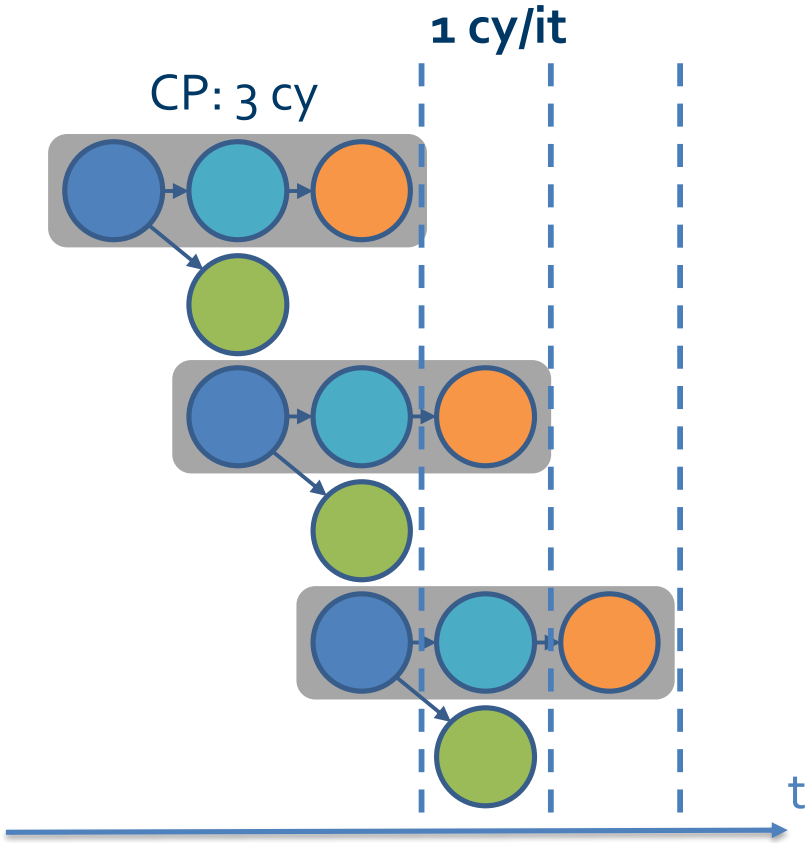

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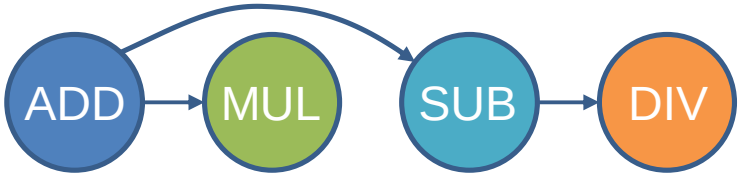

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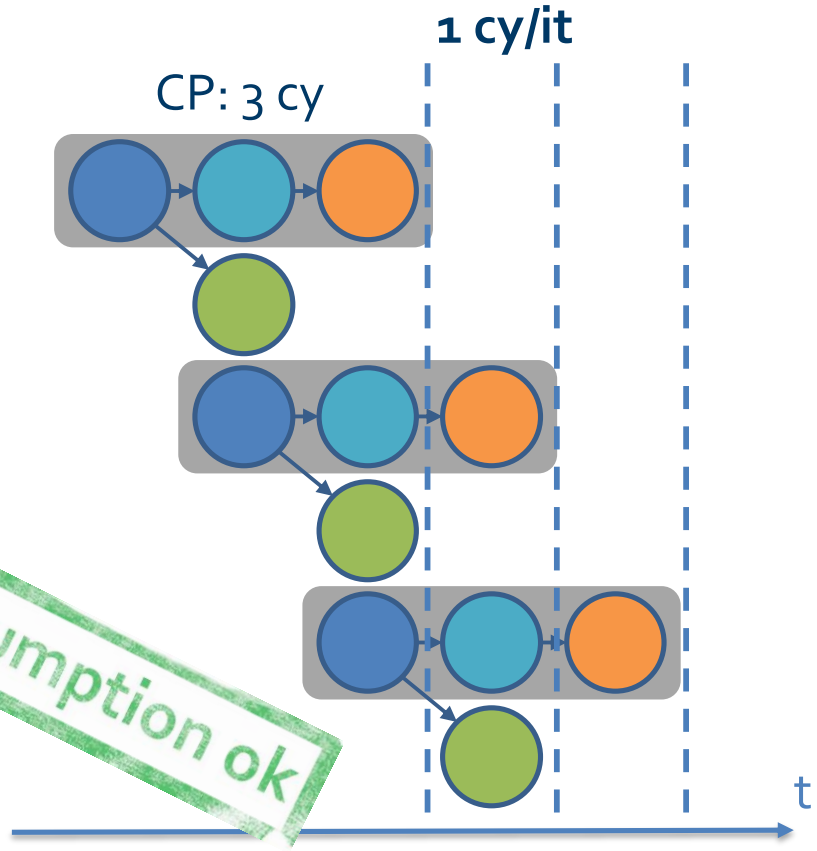

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TP assumption ok

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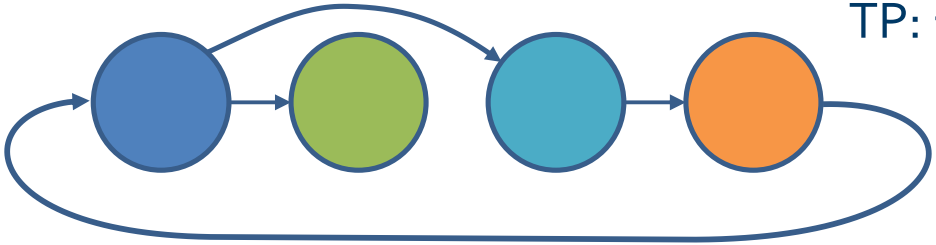
Throughput & Latency



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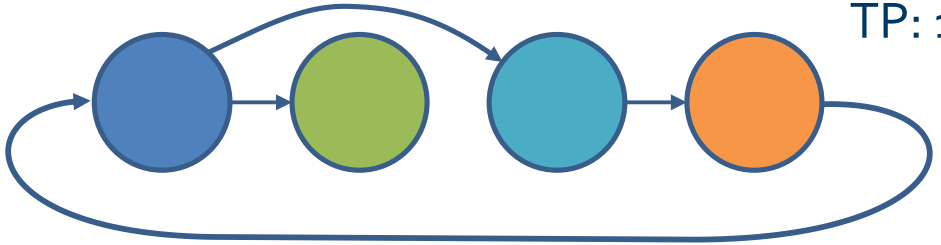

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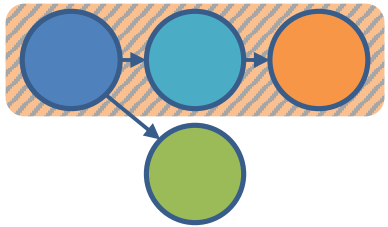

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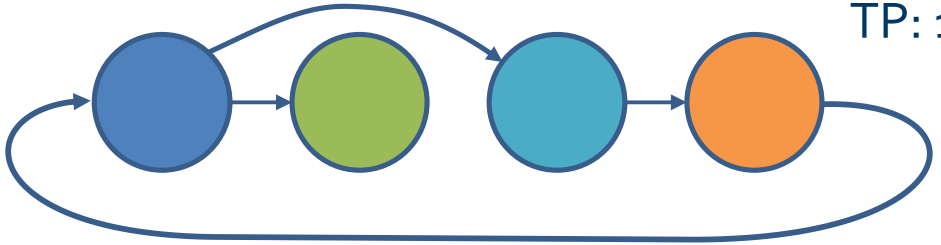

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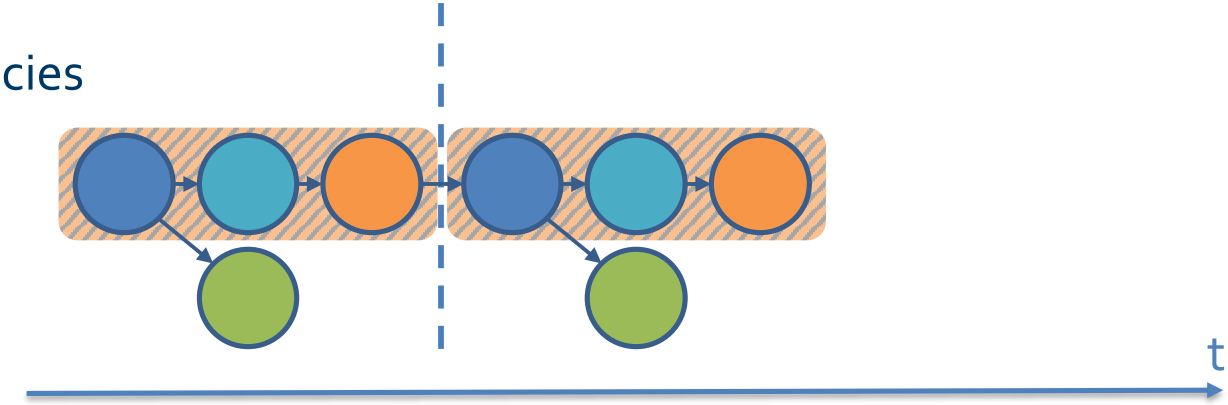

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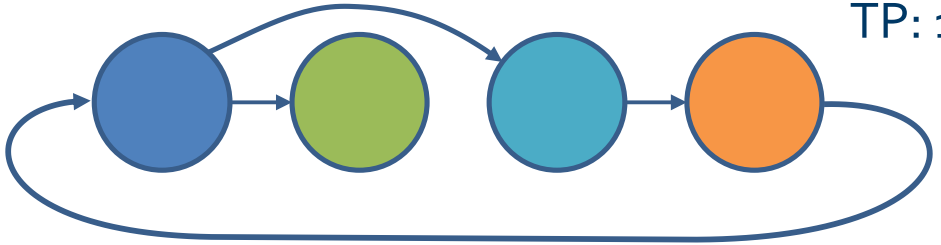

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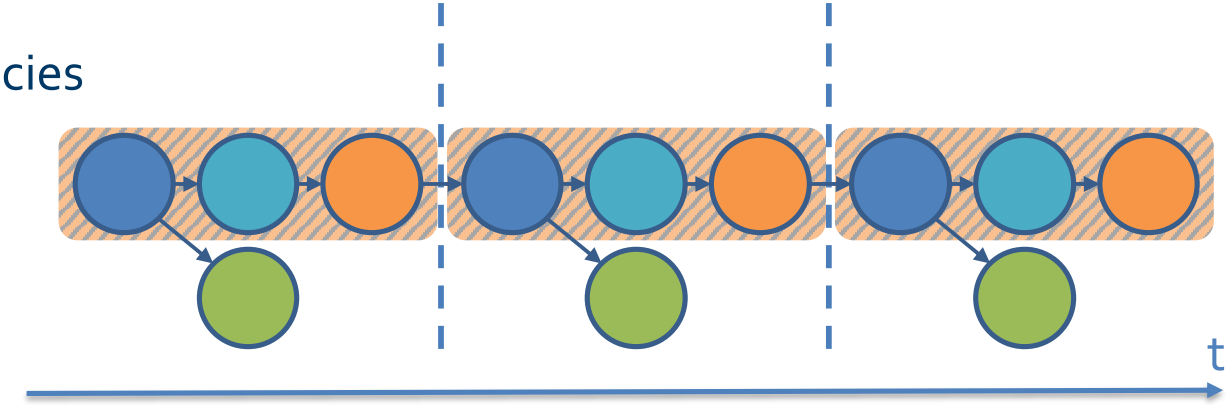

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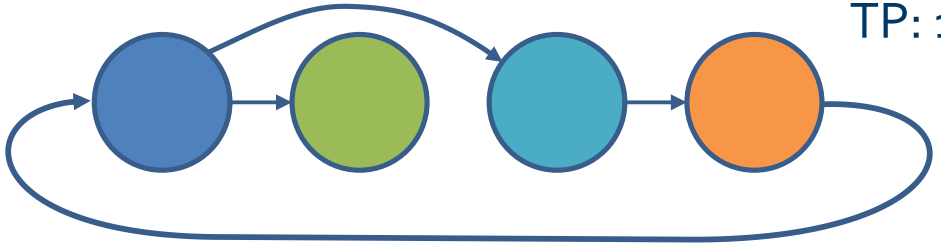

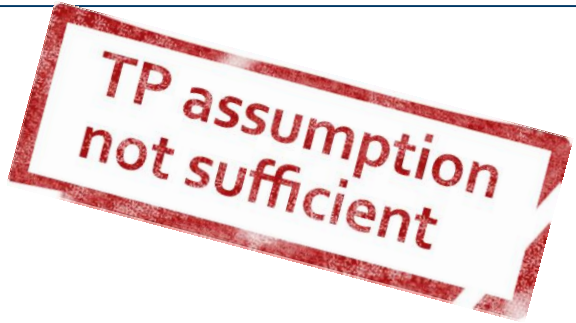

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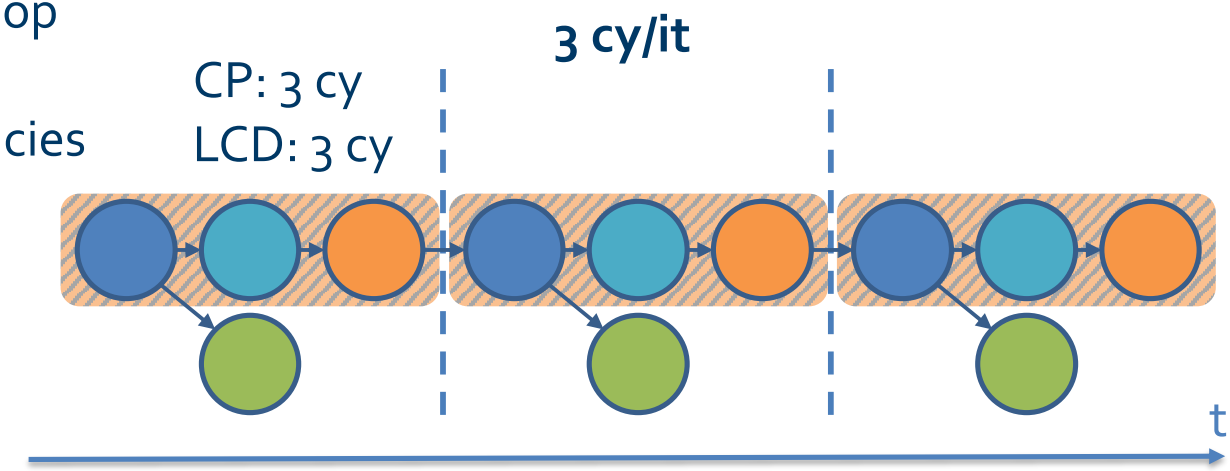

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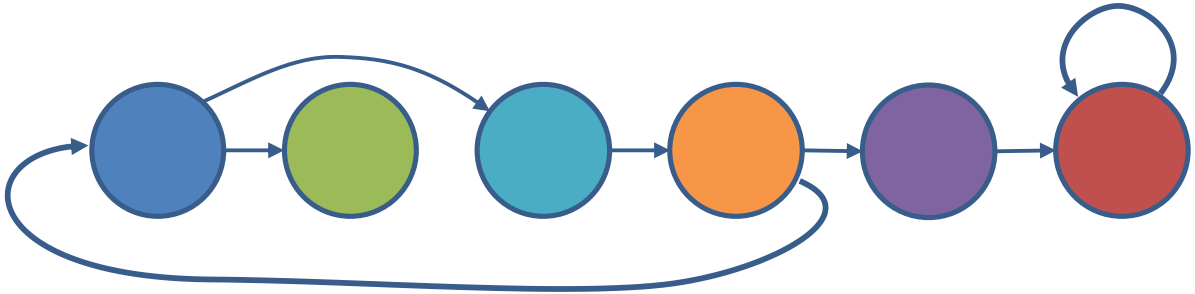

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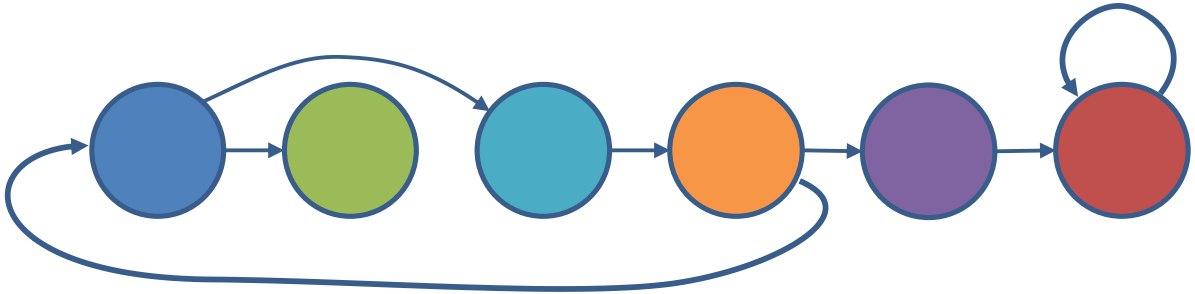

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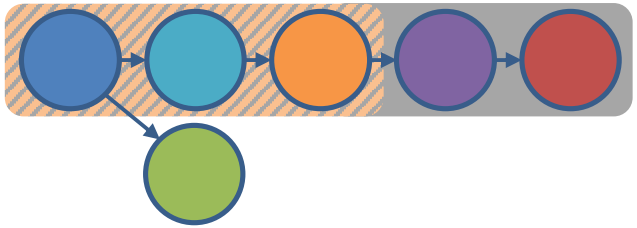

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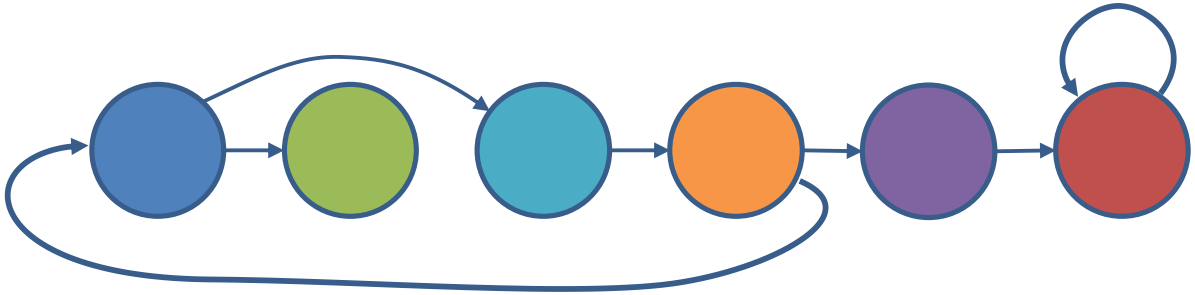

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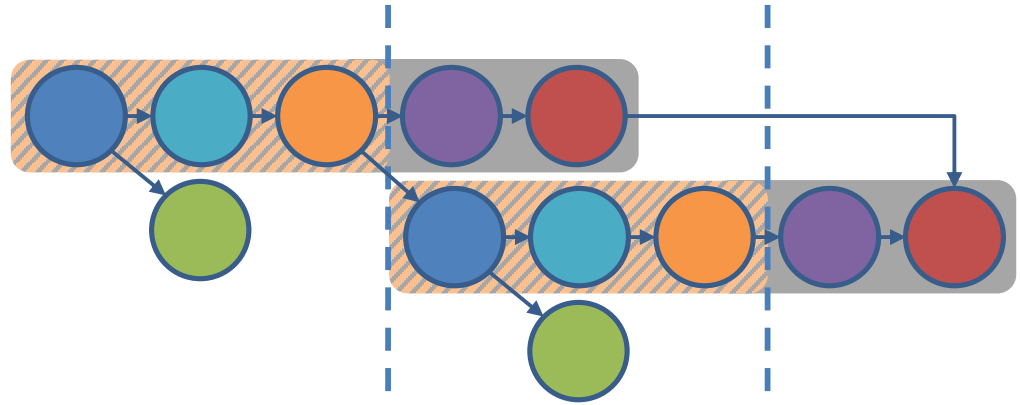

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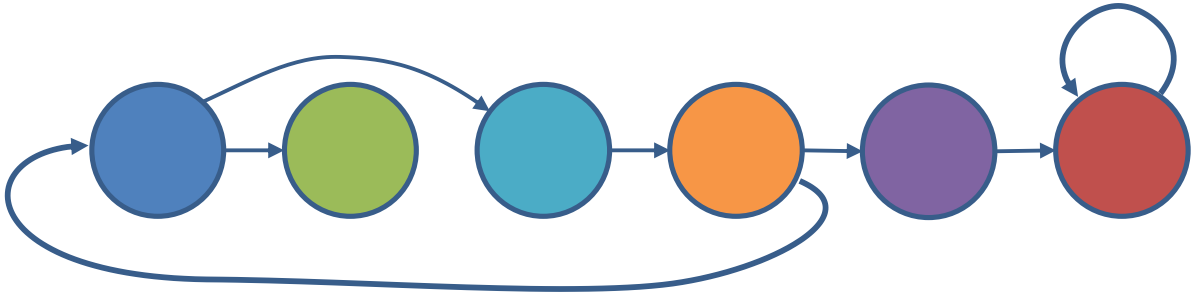

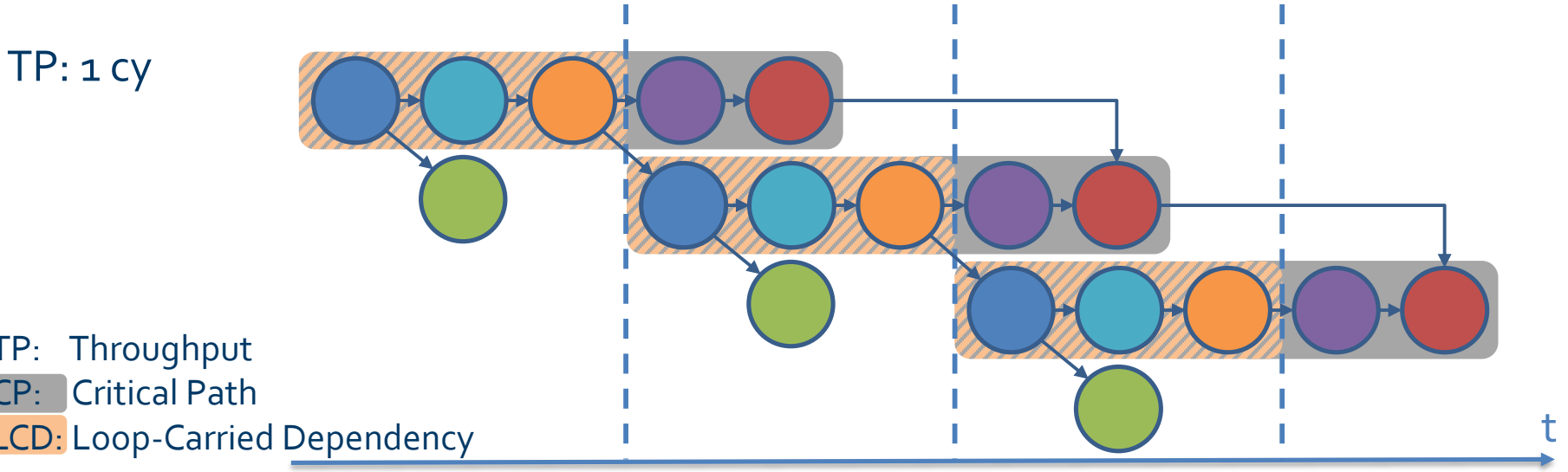

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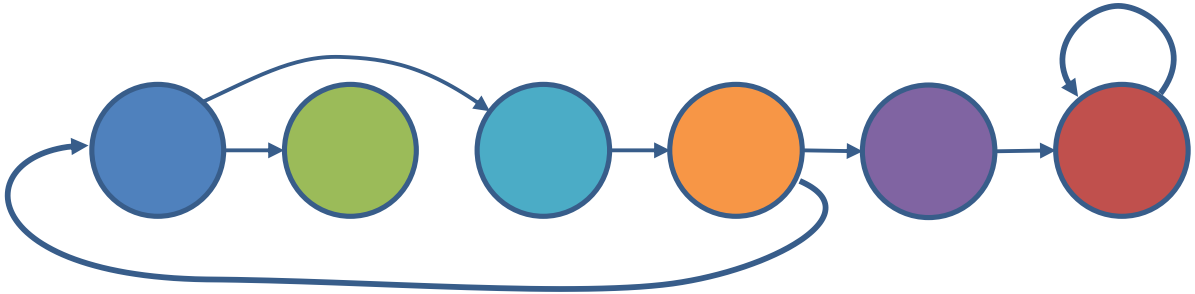

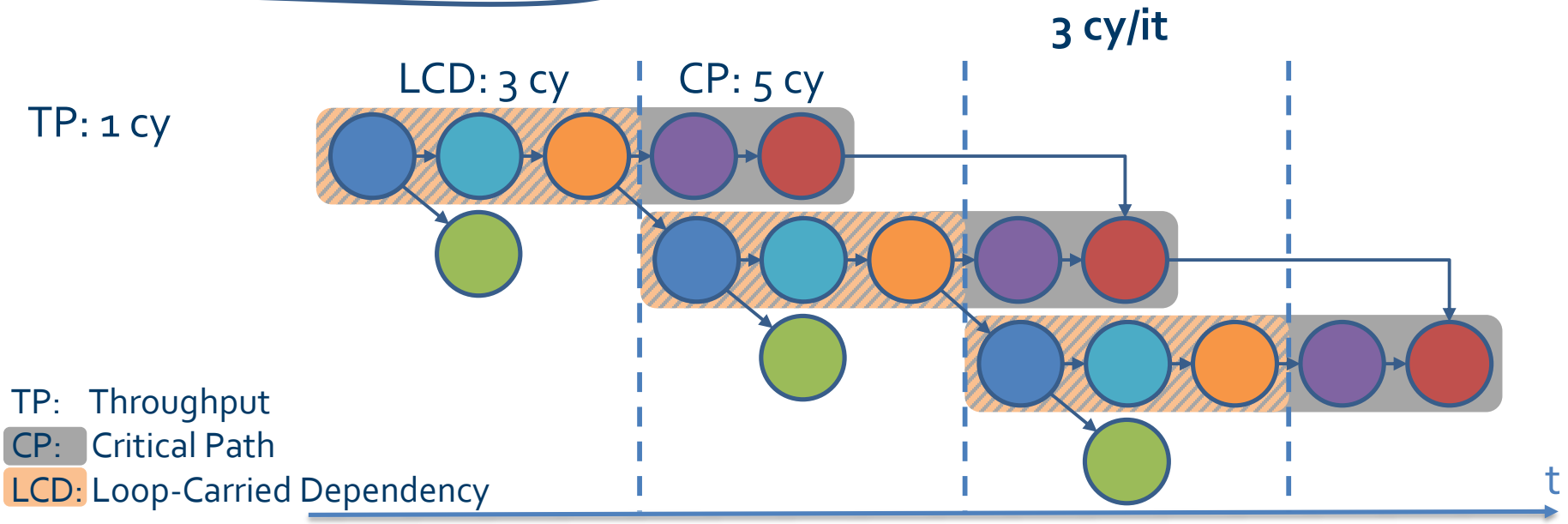

OSACA Workflow: Input – Database

Marked Assembly

x86

```
movl    $111,%ebx    #START MARKER
.byte   100,103,144  #START MARKER
.L22:
  vmovapd 0(%r13,%rax),%ymm0
  vfmadd213pd (%r14,%rax),%ymm1,%ymm0
  vmovapd %ymm0,(%r12,%rax)
  addq $32,%rax
  cmpq %rax,%r15
  jne .L22
movl    $222,%ebx    #END MARKER
.byte   100,103,144  #END MARKER
```

arm

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 mov    x1,#111      //START
 .byte  213,3,32,31 //START
 .L18:
   ldr q2, [x20, x0]
   ldr q1, [x21, x0]
   fmla v1.2d, v2.2d, v0.2d
   str q1, [x19, x0]
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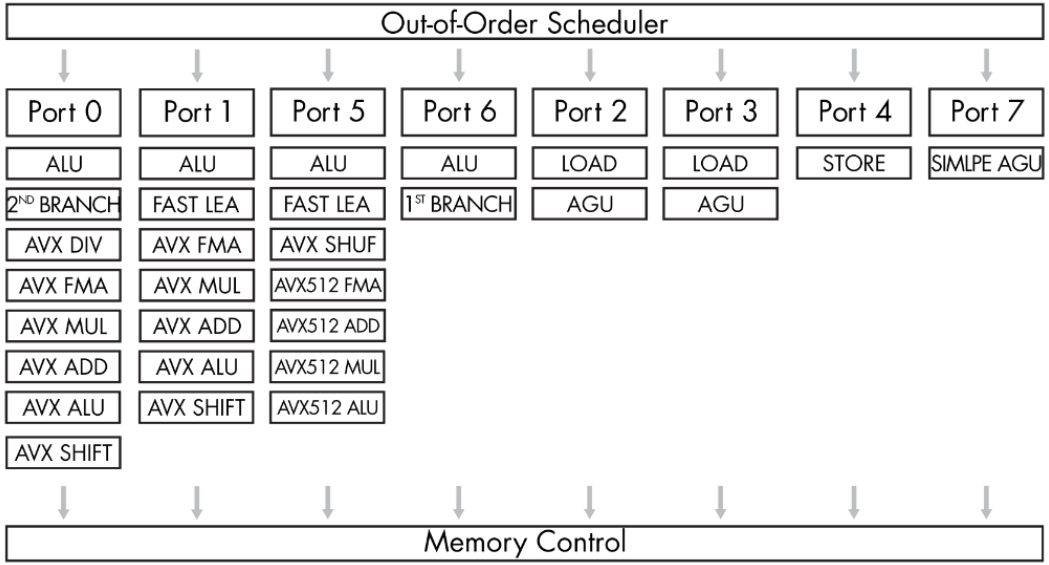
Intel Cascade Lake



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Machine Files / Databases

```
load_latency: {gpr: 4, xmm: 4, ymm: 4, zmm: 4}
load_throughput: {port_pressure: [0,0,0,0.5 ... ,0]}
- name: vfmadd213pd
  operands:
  - class: "register"
    name: "ymm"
    source: true
    destination: false
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throughput: 0.5
latency: 4    #  0  DV 1   2   D   3   D  4 5 6 7
port_pressure: [0.5,0,0.5,0.5,0.5,0.5,0.5,0,0,0,0]
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  - class: "register"
    name: "ymm"
    source: true
    destination: false
  - class: "register"
    name: "ymm"
    source: true
    destination: true
  throughput: 0.5
  latency: 4    #  0  DV 1   2   D   3   D  4 5 6 7
  port_pressure: [0.5,0,0.5,0.5,0.5,0.5,0.5,0,0,0,0]
```
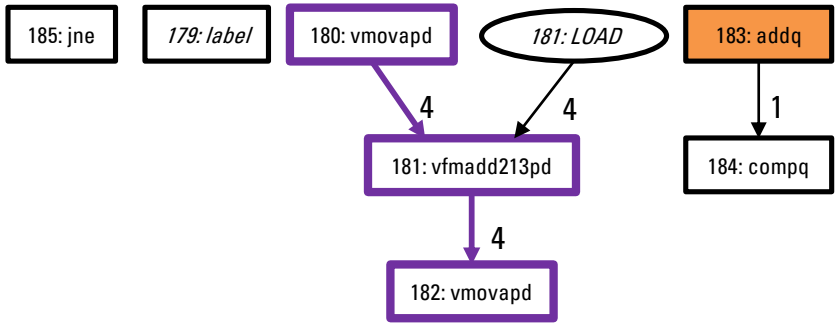
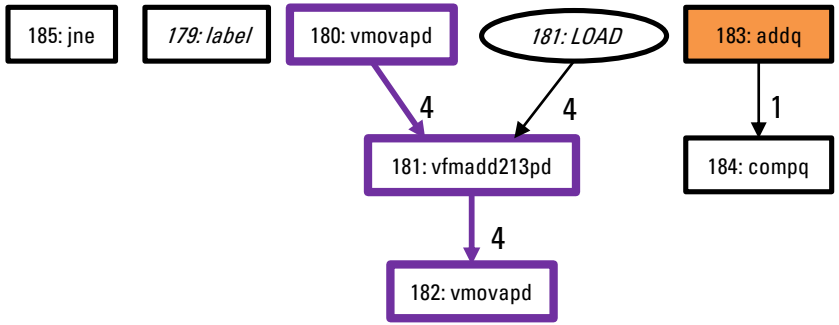

OSACA Workflow: Output

```
Combined Analysis Report
------------------------
                                 Port pressure in cycles
    |  0   - 0DV  |  1   |  2   -  2D  |  3   -  3D  |  4   |  5   |  6   |  7   ||  CP  | LCD  |
---------------------------------------------------------------------------------------------------
179 |             |      |             |             |      |      |      |      ||      |      |   .L22:
180 |             |      | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0 |      |   vmovapd 0(%r13,%rax), %ymm0
181 | 0.50        | 0.50 | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0 |      |   vfmadd213pd (%r14,%rax),%ymm1,%ymm0
182 |             |      | 0.50        | 0.50        | 1.00 |      |      |      ||  5.0 |      |   vmovapd %ymm0, (%r12,%rax)
183 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |  1.0 |   addq $32, %rax
184 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |      |   cmpq %rax, %r15
185 |             |      |             |             |      |      |      |      ||      |      | * jne .L22
     1.00         1.00   1.50   1.00   1.50   1.00   1.00   0.50   0.50          13.0    1.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
 183 |  1.0 | addq         $32, %rax                    | [183]
```



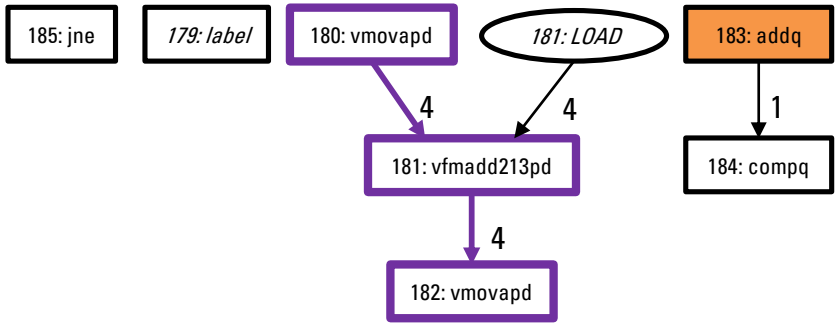
OSACA Workflow: Output

```
Combined Analysis Report
------------------------
                                 Port pressure in cycles
    |  0   - 0DV  |  1   |  2   -  2D  |  3   -  3D  |  4   |  5   |  6   |  7   ||  CP   | LCD  |
---------------------------------------------------------------------------------------------------
179 |             |      |             |             |      |      |      |      ||       |      |   .L22:
180 |             |      | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0   |      |   vmovapd 0(%r13,%rax), %ymm0
181 | 0.50        | 0.50 | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0   |      |   vfmadd213pd (%r14,%rax),%ymm1,%ymm0
182 |             |      | 0.50        | 0.50        | 1.00 |      |      |      ||  5.0   |      |   vmovapd %ymm0, (%r12,%rax)
183 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||       |  1.0 |   addq $32, %rax
184 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||       |      |   cmpq %rax, %r15
185 |             |      |             |             |      |      |      |      ||       |      | * jne .L22
     1.00         1.00   1.50   1.00   1.50   1.00   1.00   0.50   0.50         13.0    1.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
 183 |  1.0 | addq         $32, %rax                    | [183]
```



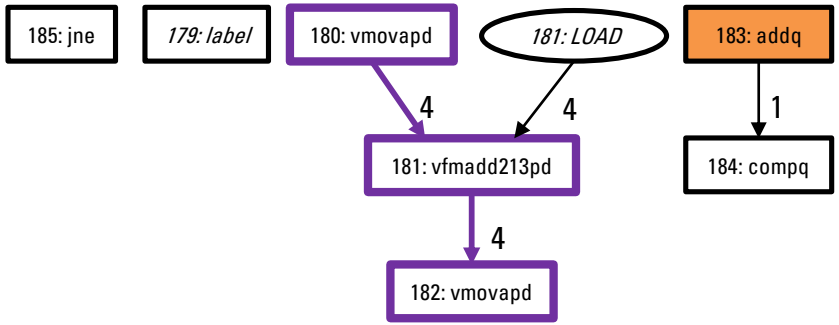
OSACA Workflow: Output

```
Combined Analysis Report
------------------------
                                 Port pressure in cycles
    |  0   - 0DV  |  1   |  2   -  2D  |  3   -  3D  |  4   |  5   |  6   |  7   ||  CP  | LCD  |
---------------------------------------------------------------------------------------------------
179 |             |      |             |             |      |      |      |      ||      |      |   .L22:
180 |             |      | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0  |      |   vmovapd 0(%r13,%rax), %ymm0
181 | 0.50        | 0.50 | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0  |      |   vfmadd213pd (%r14,%rax),%ymm1,%ymm0
182 |             |      | 0.50        | 0.50        | 1.00 |      |      |      ||  5.0  |      |   vmovapd %ymm0, (%r12,%rax)
183 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |  1.0 |   addq $32, %rax
184 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |      |   cmpq %rax, %r15
185 |             |      |             |             |      |      |      |      ||      |      | * jne .L22
     1.00         1.00   1.50   1.00   1.50   1.00   1.00   0.50   0.50         |  13.0  |  1.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
 183 |  1.0 | addq         $32, %rax                    | [183]
```



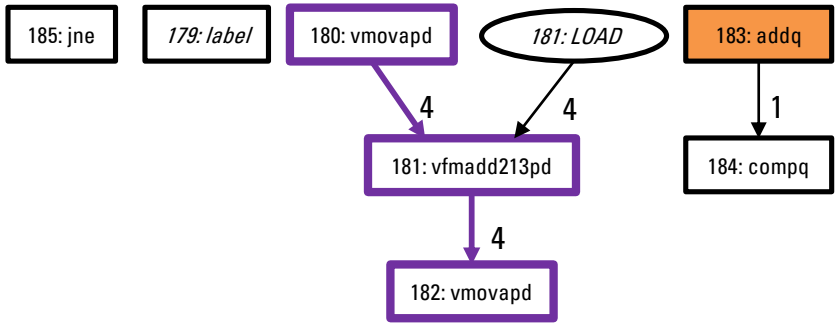
OSACA Workflow: Output

```
Combined Analysis Report
------------------------
                                 Port pressure in cycles
    |  0   - 0DV  |  1   |  2   -  2D  |  3   -  3D  |  4   |  5   |  6   |  7   ||  CP  | LCD  |
---------------------------------------------------------------------------------------------------
179 |             |      |             |             |      |      |      |      ||      |      |   .L22:
180 |             |      | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0 |      |   vmovapd 0(%r13,%rax), %ymm0
181 | 0.50        | 0.50 | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0 |      |   vfmadd213pd (%r14,%rax),%ymm1,%ymm0
182 |             |      | 0.50        | 0.50        | 1.00 |      |      |      ||  5.0 |      |   vmovapd %ymm0, (%r12,%rax)
183 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |  1.0 |   addq $32, %rax
184 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |      |   cmpq %rax, %r15
185 |             |      |             |             |      |      |      |      ||      |      | * jne .L22
      1.00          1.00   1.50   1.00   1.50   1.00   1.00   0.50   0.50          13.0   1.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
 183 |  1.0 | addq         $32, %rax                      | [183]
```



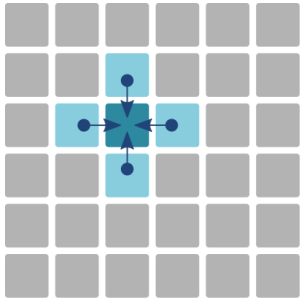
OSACA Workflow: Output

```
Combined Analysis Report
------------------------
                                 Port pressure in cycles
    |  0   - 0DV  |  1   |  2   -  2D  |  3   -  3D  |  4   |  5   |  6   |  7   ||  CP  | LCD  |
---------------------------------------------------------------------------------------------------
179 |             |      |             |             |      |      |      |      ||      |      |   .L22:
180 |             |      | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0 |      |   vmovapd 0(%r13,%rax), %ymm0
181 | 0.50        | 0.50 | 0.50   0.50 | 0.50   0.50 |      |      |      |      ||  4.0 |      |   vfmadd213pd (%r14,%rax),%ymm1,%ymm0
182 |             |      | 0.50        | 0.50        | 1.00 |      |      |      ||  5.0 |      |   vmovapd %ymm0, (%r12,%rax)
183 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |  1.0 |   addq $32, %rax
184 | 0.25        | 0.25 |             |             |      | 0.25 | 0.25 |      ||      |      |   cmpq %rax, %r15
185 |             |      |             |             |      |      |      |      ||      |      | * jne .L22
     1.00         1.00   1.50   1.00   1.50   1.00   1.00   0.50   0.50          13.0    1.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
 183 |  1.0 | addq         $32, %rax                    | [183]
```



Gauss-Seidel Method Example

- **Limited by loop-carried dependency**
- **Create code with `-Ofast`, `-funroll-loops`**
  (+ architecture specific flags)
- **Analyze for Intel Cascake Lake, AMD Zen and Marvell ThunderX2**

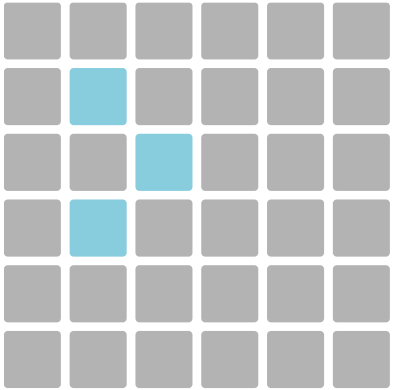


```
do it=1, itmax
  do k=1, kmax-1
    do i=1, imax-1
      phi(i,k,t0) = 0.25 * (
        phi(i,k-1,t0) + phi(i+1,k,t0) +
        phi(i,k+1,t0) + phi(i-1,k,t0))
    do
  do
do
```

Gauss-Seidel Method Example

```
  mov   x1, #111     // START MARKER
  .byte 213,3,32,31  // START MARKER
.L20:
  ldr    d31, [x15, x18, lsl 3]
  ldr    d0, [x15, 8]
  mov    x14, x15
  add    x16, x15, 24
  ldr    d2, [x15, x30, lsl 3]
  add    x15, x15, 32
  fadd   d1, d31, d0
  fadd   d3, d1, d30
  fadd   d4, d3, d2
  fmul   d5, d4, d9
  str    d5, [x14], 8
  ldr    d6, [x14, x18, lsl 3]
  ldr    d16, [x14, 8]
  add    x13, x14, 8
  ldr    d7, [x14, x30, lsl 3]
  fadd   d17, d6, d16
  fadd   d18, d17, d5
  fadd   d19, d18, d7
  fmul   d20, d19, d9
  str    d20, [x15, -24]
```

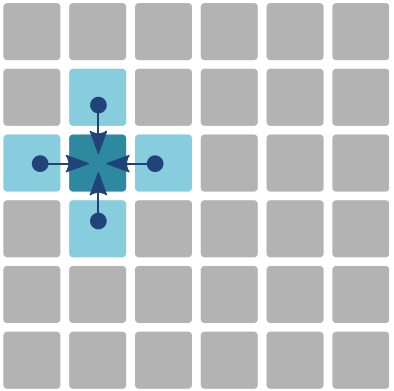
```
  ldr    d21, [x13, x18, lsl 3]
  ldr    d23, [x14, 16]
  ldr    d22, [x13, x30, lsl 3]
  fadd   d24, d21, d23
  fadd   d25, d24, d20
  fadd   d26, d25, d22
  fmul   d27, d26, d9
  str    d27, [x14, 8]
  ldr    d30, [x15]
  ldr    d28, [x16, x18, lsl 3]
  ldr    d29, [x16, x30, lsl 3]
  fadd   d31, d28, d30
  fadd   d2, d31, d27
  fadd   d0, d2, d29
  fmul   d30, d0, d9
  str    d30, [x15, -8]
  cmp    x7, x15
  bne    .L20
  mov   x1, #222      // END MARKER
  .byte 213,3,32,31   // END MARKER
```



Gauss-Seidel Method Example

```
  mov   x1, #111      // START MARKER
  .byte 213,3,32,31   // START MARKER
.L20:
  ldr    d31, [x15, x18, lsl 3]
  ldr    d0, [x15, 8]
  mov    x14, x15
  add    x16, x15, 24
  ldr    d2, [x15, x30, lsl 3]
  add    x15, x15, 32
  fadd   d1, d31, d0
  fadd   d3, d1, d30
  fadd   d4, d3, d2
  fmul   d5, d4, d9
  str    d5, [x14], 8
  ldr    d6, [x14, x18, lsl 3]
  ldr    d16, [x14, 8]
  add    x13, x14, 8
  ldr    d7, [x14, x30, lsl 3]
  fadd   d17, d6, d16
  fadd   d18, d17, d5
  fadd   d19, d18, d7
  fmul   d20, d19, d9
  str    d20, [x15, -24]
```

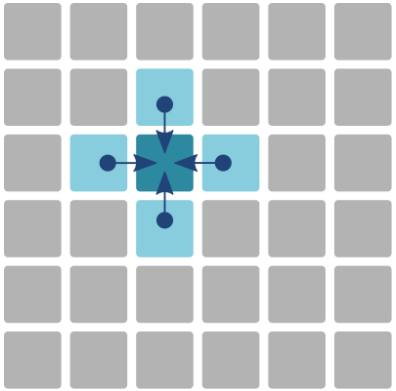
```
  ldr    d21, [x13, x18, lsl 3]
  ldr    d23, [x14, 16]
  ldr    d22, [x13, x30, lsl 3]
  fadd   d24, d21, d23
  fadd   d25, d24, d20
  fadd   d26, d25, d22
  fmul   d27, d26, d9
  str    d27, [x14, 8]
  ldr    d30, [x15]
  ldr    d28, [x16, x18, lsl 3]
  ldr    d29, [x16, x30, lsl 3]
  fadd   d31, d28, d30
  fadd   d2, d31, d27
  fadd   d0, d2, d29
  fmul   d30, d0, d9
  str    d30, [x15, -8]
  cmp    x7, x15
  bne    .L20
  mov   x1, #222      // END MARKER
  .byte 213,3,32,31   // END MARKER
```



Gauss-Seidel Method Example

```
  mov   x1, #111     // START MARKER
  .byte 213,3,32,31  // START MARKER
.L20:
  ldr    d31, [x15, x18, lsl 3]
  ldr    d0, [x15, 8]
  mov    x14, x15
  add    x16, x15, 24
  ldr    d2, [x15, x30, lsl 3]
  add    x15, x15, 32
  fadd   d1, d31, d0
  fadd   d3, d1, d30
  fadd   d4, d3, d2
  fmul   d5, d4, d9
  str    d5, [x14], 8
  ldr    d6, [x14, x18, lsl 3]
  ldr    d16, [x14, 8]
  add    x13, x14, 8
  ldr    d7, [x14, x30, lsl 3]
  fadd   d17, d6, d16
  fadd   d18, d17, d5
  fadd   d19, d18, d7
  fmul   d20, d19, d9
  str    d20, [x15, -24]
```

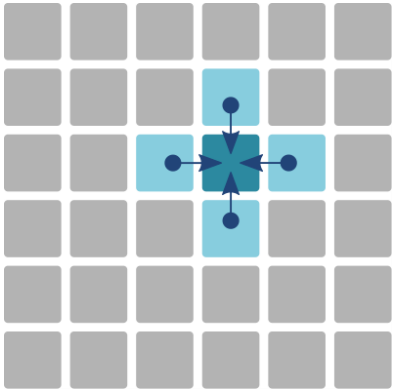
```
  ldr    d21, [x13, x18, lsl 3]
  ldr    d23, [x14, 16]
  ldr    d22, [x13, x30, lsl 3]
  fadd   d24, d21, d23
  fadd   d25, d24, d20
  fadd   d26, d25, d22
  fmul   d27, d26, d9
  str    d27, [x14, 8]
  ldr    d30, [x15]
  ldr    d28, [x16, x18, lsl 3]
  ldr    d29, [x16, x30, lsl 3]
  fadd   d31, d28, d30
  fadd   d2, d31, d27
  fadd   d0, d2, d29
  fmul   d30, d0, d9
  str    d30, [x15, -8]
  cmp    x7, x15
  bne    .L20
  mov   x1, #222      // END MARKER
  .byte 213,3,32,31   // END MARKER
```



Gauss-Seidel Method Example

```
  mov   x1, #111     // START MARKER
  .byte 213,3,32,31  // START MARKER
.L20:
  ldr    d31, [x15, x18, lsl 3]
  ldr    d0, [x15, 8]
  mov    x14, x15
  add    x16, x15, 24
  ldr    d2, [x15, x30, lsl 3]
  add    x15, x15, 32
  fadd   d1, d31, d0
  fadd   d3, d1, d30
  fadd   d4, d3, d2
  fmul   d5, d4, d9
  str    d5, [x14], 8
  ldr    d6, [x14, x18, lsl 3]
  ldr    d16, [x14, 8]
  add    x13, x14, 8
  ldr    d7, [x14, x30, lsl 3]
  fadd   d17, d6, d16
  fadd   d18, d17, d5
  fadd   d19, d18, d7
  fmul   d20, d19, d9
  str    d20, [x15, -24]
```

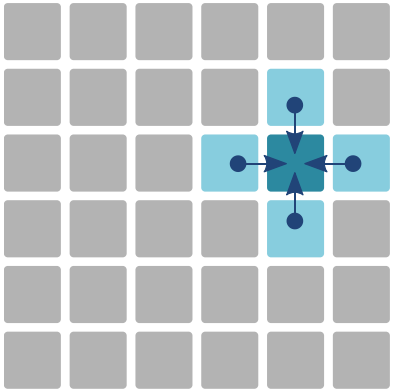
```
  ldr    d21, [x13, x18, lsl 3]
  ldr    d23, [x14, 16]
  ldr    d22, [x13, x30, lsl 3]
  fadd   d24, d21, d23
  fadd   d25, d24, d20
  fadd   d26, d25, d22
  fmul   d27, d26, d9
  str    d27, [x14, 8]
  ldr    d30, [x15]
  ldr    d28, [x16, x18, lsl 3]
  ldr    d29, [x16, x30, lsl 3]
  fadd   d31, d28, d30
  fadd   d2, d31, d27
  fadd   d0, d2, d29
  fmul   d30, d0, d9
  str    d30, [x15, -8]
  cmp    x7, x15
  bne    .L20
  mov   x1, #222      // END MARKER
  .byte 213,3,32,31   // END MARKER
```



Gauss-Seidel Method Example

```
  mov   x1, #111     // START MARKER
  .byte 213,3,32,31  // START MARKER
.L20:
  ldr    d31, [x15, x18, lsl 3]
  ldr    d0, [x15, 8]
  mov    x14, x15
  add    x16, x15, 24
  ldr    d2, [x15, x30, lsl 3]
  add    x15, x15, 32
  fadd   d1, d31, d0
  fadd   d3, d1, d30
  fadd   d4, d3, d2
  fmul   d5, d4, d9
  str    d5, [x14], 8
  ldr    d6, [x14, x18, lsl 3]
  ldr    d16, [x14, 8]
  add    x13, x14, 8
  ldr    d7, [x14, x30, lsl 3]
  fadd   d17, d6, d16
  fadd   d18, d17, d5
  fadd   d19, d18, d7
  fmul   d20, d19, d9
  str    d20, [x15, -24]
```

```
  ldr    d21, [x13, x18, lsl 3]
  ldr    d23, [x14, 16]
  ldr    d22, [x13, x30, lsl 3]
  fadd   d24, d21, d23
  fadd   d25, d24, d20
  fadd   d26, d25, d22
  fmul   d27, d26, d9
  str    d27, [x14, 8]
  ldr    d30, [x15]
  ldr    d28, [x16, x18, lsl 3]
  ldr    d29, [x16, x30, lsl 3]
  fadd   d31, d28, d30
  fadd   d2, d31, d27
  fadd   d0, d2, d29
  fmul   d30, d0, d9
  str    d30, [x15, -8]
  cmp    x7, x15
  bne    .L20
  mov   x1, #222      // END MARKER
  .byte 213,3,32,31   // END MARKER
```



Gauss-Seidel Method Example – Output

```
                                Port pressure in cycles
    |  0   - 0DV  |  1   - 1DV  |  2   |  3   |  4   |  5   ||  CP   | LCD  |
----------------------------------------------------------------------------
520 |             |             |      |      |      |      ||       |      |                .L20:
521 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |    ldr    d31, [x15, x18, lsl 3]
522 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d0, [x15, 8]
523 |  0.50       |  0.50       |      |      |      |      ||       |      |    mov    x14, x15
524 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |    add    x16, x15, 24
525 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d2, [x15, x30, lsl 3]
526 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |    add    x15, x15, 32
527 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |    fadd   d1, d31, d0
528 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d3, d1, d30
529 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d4, d3, d2
530 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fmul   d5, d4, d9
531 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |    str    d5, [x14], 8
532 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |    ldr    d6, [x14, x18, lsl 3]
533 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d16, [x14, 8]
534 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |    add    x13, x14, 8
535 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d7, [x14, x30, lsl 3]
536 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |    fadd   d17, d6, d16
537 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d18, d17, d5
538 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d19, d18, d7
539 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fmul   d20, d19, d9
540 |             |             |      | 0.50 | 0.50 | 1.00 ||       |      |    str    d20, [x15, -24]
541 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d21, [x13, x18, lsl 3]
542 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d23, [x14, 16]
543 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d22, [x13, x30, lsl 3]
544 |  0.50       |  0.50       |      |      |      |      ||       |      |    fadd   d24, d21, d23
545 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d25, d24, d20
546 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d26, d25, d22
547 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fmul   d27, d26, d9
548 |             |             |      | 0.50 | 0.50 | 1.00 ||       |      |    str    d27, [x14, 8]
549 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d30, [x15]
550 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d28, [x16, x18, lsl 3]
551 |             |             |      | 0.50 | 0.50 |      ||       |      |    ldr    d29, [x16, x30, lsl 3]
552 |  0.50       |  0.50       |      |      |      |      ||       |      |    fadd   d31, d28, d30
553 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d2, d31, d27
554 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fadd   d0, d2, d29
555 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |    fmul   d30, d0, d9
556 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |    str    d30, [x15, -8]
557 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |    cmp    x7, x15
558 |             |             |      |      |      |      ||       |      | * bne     .L20

      9.83          9.83          1.33   8.00   8.00   4.00   100.0   72.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
526 |  1.0 | add    x15, x15, 32                | [526]
555 | 72.0 | fmul    d30, d0, d9                | [528, 529, 530, 537, 538, 539, 545, 546, 547, 553, 554, 555]
```

Gauss-Seidel Method Example – Output

```
                                Port pressure in cycles
    |  0   - 0DV  |  1   - 1DV  |  2   |  3   |  4   |  5   ||  CP   | LCD  |
---------------------------------------------------------------------------------
520 |             |             |      |      |      |      ||       |      |  .L20:
521 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |  ldr    d31, [x15, x18, lsl 3]
522 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d0, [x15, 8]
523 |  0.50       |  0.50       |      |      |      |      ||       |      |  mov    x14, x15
524 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |  add    x16, x15, 24
525 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d2, [x15, x30, lsl 3]
526 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |  add    x15, x15, 32
527 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |  fadd   d1, d31, d0
528 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d3, d1, d30
529 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d4, d3, d2
530 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d5, d4, d9
531 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |  str    d5, [x14], 8
532 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |  ldr    d6, [x14, x18, lsl 3]
533 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d16, [x14, 8]
534 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |  add    x13, x14, 8
535 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d7, [x14, x30, lsl 3]
536 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |  fadd   d17, d6, d16
537 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d18, d17, d5
538 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d19, d18, d7
539 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d20, d19, d9
540 |             |             |      | 0.50 | 0.50 | 1.00 ||       |      |  str    d20, [x15, -24]
541 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d21, [x13, x18, lsl 3]
542 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d23, [x14, 16]
543 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d22, [x13, x30, lsl 3]
544 |  0.50       |  0.50       |      |      |      |      ||       |      |  fadd   d24, d21, d23
545 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d25, d24, d20
546 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d26, d25, d22
547 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d27, d26, d9
548 |             |             |      | 0.50 | 0.50 | 1.00 ||       |      |  str    d27, [x14, 8]
549 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d30, [x15]
550 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d28, [x16, x18, lsl 3]
551 |             |             |      | 0.50 | 0.50 |      ||       |      |  ldr    d29, [x16, x30, lsl 3]
552 |  0.50       |  0.50       |      |      |      |      ||       |      |  fadd   d31, d28, d30
553 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d2, d31, d27
554 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d0, d2, d29
555 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d30, d0, d9
556 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |  str    d30, [x15, -8]
557 |  0.33       |  0.33       | 0.33 |      |      |      ||       |      |  cmp    x7, x15
558 |             |             |      |      |      |      ||       |      |* bne    .L20
---------------------------------------------------------------------------------
    9.83          9.83          1.33   8.00   8.00   4.00   100.0   72.0

Loop-Carried Dependencies Analysis Report
-----------------------------------------
526 |  1.0 | add    x15, x15, 32                | [526]
555 | 72.0 | fmul    d30, d0, d9                | [528, 529, 530, 537, 538, 539, 545, 546, 547, 553, 554, 555]
```

Block Throughput	2.46 cy

Gauss-Seidel Method Example – Output

```
                                Port pressure in cycles
    |  0   - 0DV  |  1   - 1DV  |  2   |  3   |  4   |  5   ||  CP  | LCD  |
---------------------------------------------------------------------------
520 |             |             |      |      |      |      ||      |      |                .L20:
521 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |  ldr    d31, [x15, x18, lsl 3]
522 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d0, [x15, 8]
523 |  0.50       |  0.50       |      |      |      |      ||      |      |  mov    x14, x15
524 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  add    x16, x15, 24
525 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d2, [x15, x30, lsl 3]
526 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  add    x15, x15, 32
527 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |  fadd   d1, d31, d0
528 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d3, d1, d30
529 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d4, d3, d2
530 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d5, d4, d9
531 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |  str    d5, [x14], 8
532 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |  ldr    d6, [x14, x18, lsl 3]
533 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d16, [x14, 8]
534 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  add    x13, x14, 8
535 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d7, [x14, x30, lsl 3]
536 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |  fadd   d17, d6, d16
537 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d18, d17, d5
538 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d19, d18, d7
539 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d20, d19, d9
540 |             |             |      | 0.50 | 0.50 | 1.00 ||      |      |  str    d20, [x15, -24]
541 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d21, [x13, x18, lsl 3]
542 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d23, [x14, 16]
543 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d22, [x13, x30, lsl 3]
544 |  0.50       |  0.50       |      |      |      |      ||      |      |  fadd   d24, d21, d23
545 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d25, d24, d20
546 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d26, d25, d22
547 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d27, d26, d9
548 |             |             |      | 0.50 | 0.50 | 1.00 ||      |      |  str    d27, [x14, 8]
549 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d30, [x15]
550 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d28, [x16, x18, lsl 3]
551 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d29, [x16, x30, lsl 3]
552 |  0.50       |  0.50       |      |      |      |      ||      |      |  fadd   d31, d28, d30
553 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d2, d31, d27
554 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d0, d2, d29
555 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d30, d0, d9
556 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |  str    d30, [x15, -8]
557 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  cmp    x7, x15
558 |             |             |      |      |      |      ||      |      |* bne    .L20
    |  9.83       |  9.83       | 1.33 | 8.00 | 8.00 | 4.00 || 100  | 72.0 |

Loop-Carried Dependencies Analysis Report
-----------------------------------------
526 |  1.0 | add    x15, x15, 32                | [526]
555 | 72.0 | fmul    d30, d0, d9                | [528, 529, 530, 537, 538, 539, 545, 546, 547, 553, 554, 555]
```

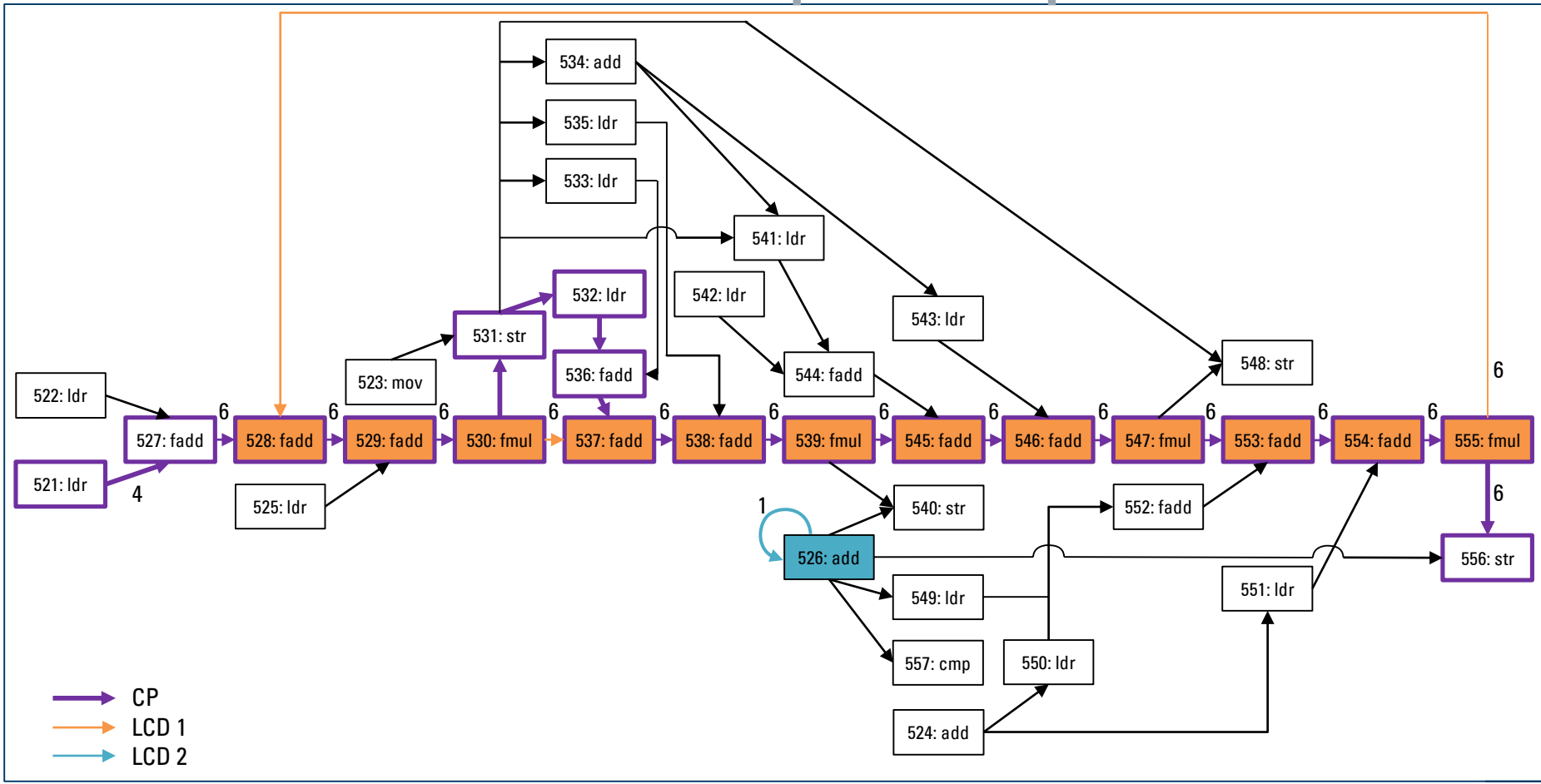
Block Throughput	2.46 cy
Critical Path	25.0 cy

Gauss-Seidel Method Example – Output

```
                                Port pressure in cycles
    |  0   - 0DV  |  1   - 1DV  |  2   |  3   |  4   |  5   ||  CP  | LCD  |
---------------------------------------------------------------------------
520 |             |             |      |      |      |      ||      |      |  .L20:
521 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |  ldr    d31, [x15, x18, lsl 3]
522 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d0, [x15, 8]
523 |  0.50       |  0.50       |      |      |      |      ||      |      |  mov    x14, x15
524 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  add    x16, x15, 24
525 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d2, [x15, x30, lsl 3]
526 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  add    x15, x15, 32
527 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |  fadd   d1, d31, d0
528 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d3, d1, d30
529 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d4, d3, d2
530 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d5, d4, d9
531 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |  str    d5, [x14], 8
532 |             |             |      | 0.50 | 0.50 |      ||  4.0  |      |  ldr    d6, [x14, x18, lsl 3]
533 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d16, [x14, 8]
534 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  add    x13, x14, 8
535 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d7, [x14, x30, lsl 3]
536 |  0.50       |  0.50       |      |      |      |      ||  6.0  |      |  fadd   d17, d6, d16
537 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d18, d17, d5
538 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d19, d18, d7
539 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d20, d19, d9
540 |             |             |      | 0.50 | 0.50 | 1.00 ||      |      |  str    d20, [x15, -24]
541 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d21, [x13, x18, lsl 3]
542 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d23, [x14, 16]
543 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d22, [x13, x30, lsl 3]
544 |  0.50       |  0.50       |      |      |      |      ||      |      |  fadd   d24, d21, d23
545 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d25, d24, d20
546 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d26, d25, d22
547 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d27, d26, d9
548 |             |             |      | 0.50 | 0.50 | 1.00 ||      |      |  str    d27, [x14, 8]
549 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d30, [x15]
550 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d28, [x16, x18, lsl 3]
551 |             |             |      | 0.50 | 0.50 |      ||      |      |  ldr    d29, [x16, x30, lsl 3]
552 |  0.50       |  0.50       |      |      |      |      ||      |      |  fadd   d31, d28, d30
553 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d2, d31, d27
554 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fadd   d0, d2, d29
555 |  0.50       |  0.50       |      |      |      |      ||  6.0  |  6.0 |  fmul   d30, d0, d9
556 |             |             |      | 0.50 | 0.50 | 1.00 ||  4.0  |      |  str    d30, [x15, -8]
557 |  0.33       |  0.33       | 0.33 |      |      |      ||      |      |  cmp    x7, x15
558 |             |             |      |      |      |      ||      |      |* bne    .L20
    |  9.83       |  9.83       | 1.33 | 8.00 | 8.00 | 4.00 ||  100 |  72  |

Loop-Carried Dependencies Analysis Report
-----------------------------------------
526 |  1.0 | add    x15, x15, 32              | [526]
555 | 72.0 | fmul   d30, d0, d9               | [528, 529, 530, 537, 538, 539, 545, 546, 547, 553, 554, 555]
```

Block Throughput	2.46 cy
Critical Path	25.0 cy
Loop-Carried Dep.	18.0 cy

Gauss-Seidel Method Example – Output



Results & Comparison

Architecture	Unroll factor	Measured		Prediction [cy/it]								
				OSACA			IACA			LLVM-MCA		
		MLUP/s	cy/it	TP	LCD	CP	TP	LCD	CP	TP	LCD	CP
Intel Cascade Lake X	4x	178.3	14.02	2.19	14.0	18.0	2.0 (14.0)			2.0	14.75	19.0
AMD Zen	4x	194.4	11.83	2.0	11.5	15.0				3.0	18.0	24.0
Marvell ThunderX2	4x	118.9	18.50	2.46	18.0	25.0						

Results & Comparison

Architecture	Unroll factor	Measured		Prediction [cy/it]								
				OSACA			IACA			LLVM-MCA		
		MLUP/s	cy/it	TP	LCD	CP	TP	LCD	CP	TP	LCD	CP
Intel Cascade Lake X	4x	178.3	14.02	2.19	14.0	18.0	2.0 (14.0)			2.0	14.75	19.0
AMD Zen	4x	194.4	11.83	2.0	11.5	15.0				3.0	18.0	24.0
Marvell ThunderX2	4x	118.9	18.50	2.46	18.0	25.0						

Results & Comparison

Architecture	Unroll factor	Measured		Prediction [cy/it]								
				OSACA			IACA			LLVM-MCA		
		MLUP/s	cy/it	TP	LCD	CP	TP	LCD	CP	TP	LCD	CP
Intel Cascade Lake X	4x	178.3	14.02	2.19	14.0	18.0	2.0 (14.0)			2.0	14.75	19.0
AMD Zen	4x	194.4	11.83	2.0	11.5	15.0				3.0	18.0	24.0
Marvell ThunderX2	4x	118.9	18.50	2.46	18.0	25.0						

Results & Comparison

Architecture	Unroll factor	Measured		Prediction [cy/it]								
				OSACA			IACA			LLVM-MCA		
		MLUP/s	cy/it	TP	LCD	CP	TP	LCD	CP	TP	LCD	CP
Intel Cascade Lake X	4x	178.3	14.02	2.19	14.0	18.0	2.0 (14.0)			2.0	14.75	19.0
AMD Zen	4x	194.4	11.83	2.0	11.5	15.0				3.0	18.0	24.0
Marvell ThunderX2	4x	118.9	18.50	2.46	18.0	25.0						

Summary – OSACA

- Automatic extraction, throughput and critical path analysis
- Cross-platform (Intel, AMD, ARM)
- Accurate predictions
- Open Source
- Allows architectural exploration

Future Work

- Support of hidden dependencies
- More precise LCD analysis
- Support new micro-architectures (Zen 2, Power 9, …)
- More precise latency analysis for FMA instructions
- Considering ROB, register renaming, retirement, …
- Optimally balanced port utilization

Future Work

- Support of hidden dependencies
- More precise LCD analysis
- Support new micro-architectures (Zen 2, Power 9, …)
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- Optimally balanced port utilization 

Future Work

- Support of hidden dependencies
- More precise LCD analysis
- Support new micro-architectures (Zen 2, Power 9, …)
- More precise latency analysis for FMA instructions
- Considering ROB, register renaming, retirement, …
- Optimally balanced port utilization ✓

github.com/RRZE-HPC/OSACA

OSACA

Open Source Architecture Code Analyzer

Reproduce at: https://github.com/RRZE-HPC/OSACA-CP-2019/